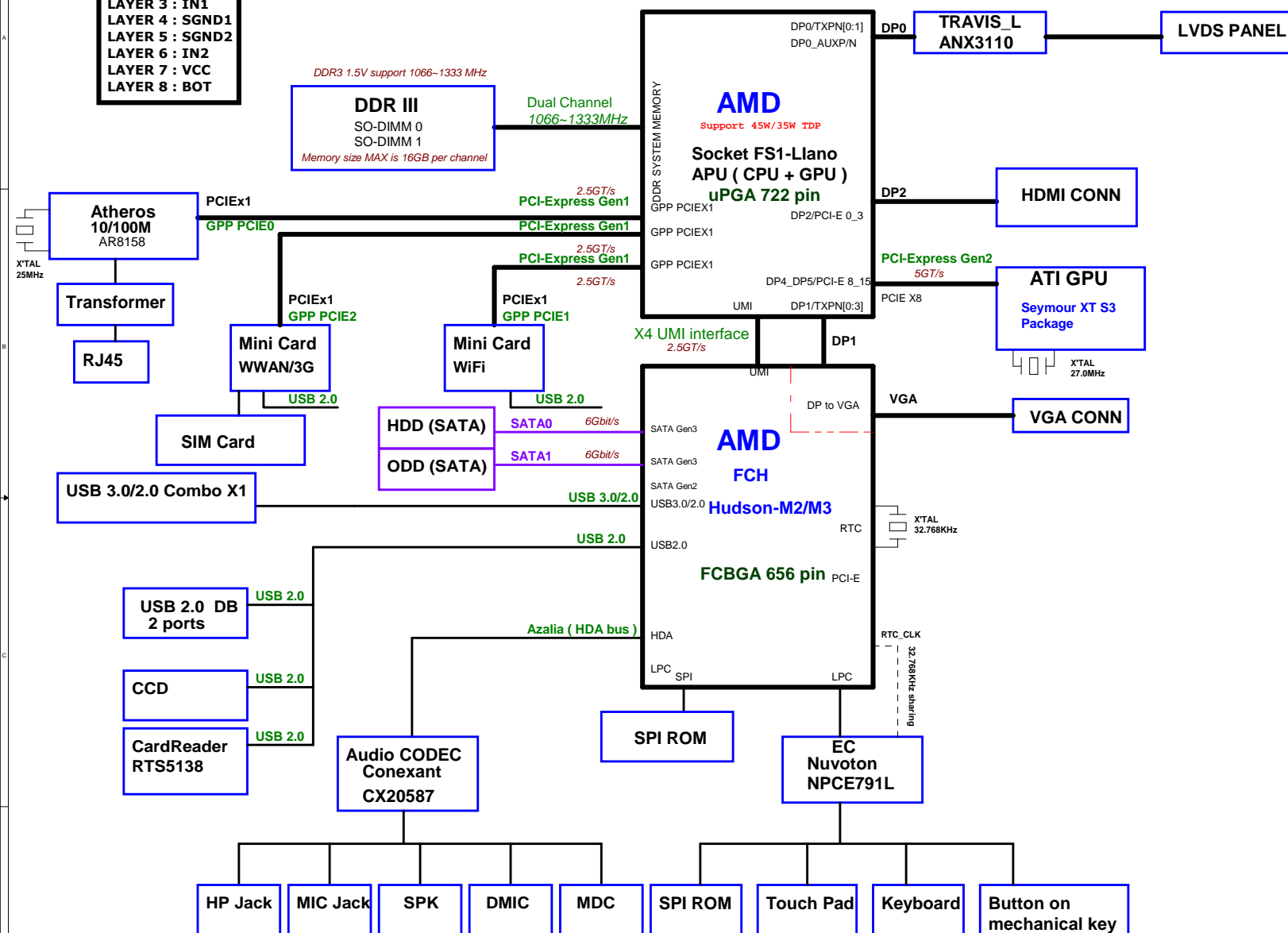


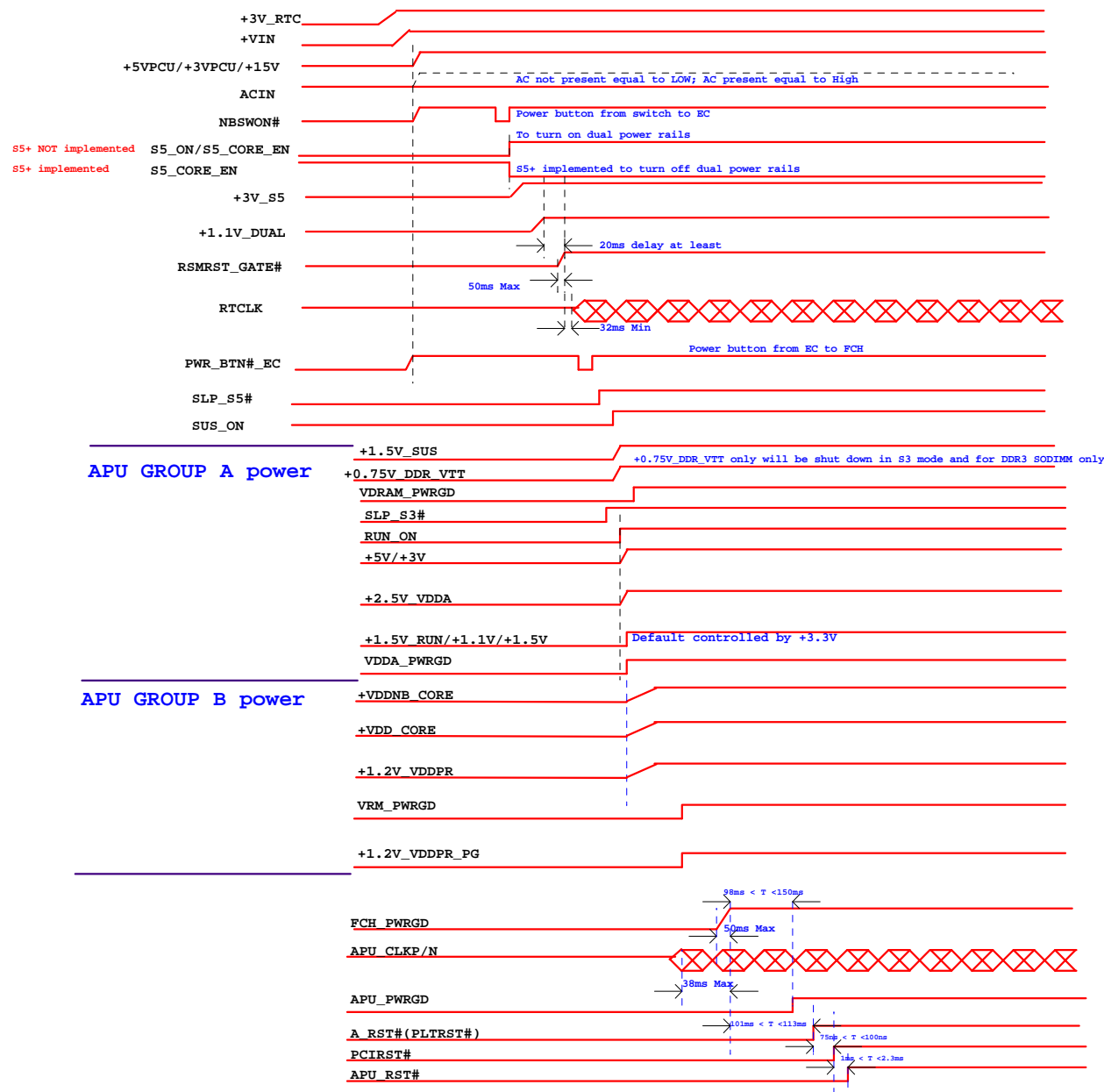
PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : SGND1
LAYER 5 : SGND2
LAYER 6 : IN2
LAYER 7 : VCC
LAYER 8 : BOT

BLOCK DIAGRAM



BLF/BLFD Power On Sequence: S5 > S0



APU Power on sequence required:

Llano APU:

- 1.Group A (+1.5V_SUS, +2.5V_VDDA) ramp before Group B (+VDD_CORE, +VDDNB_CORE, +1.2V_VDDPR)

HUDSON-M2/M3:

- 1.+3V_S5 ramp before +1.1V_DUAL
- 2.+3V ramp before +1.1V
- 3.+3V_RTC must ramp at least 5 secs before the +3V_S5

Seymour XT S3 package Power-on sequence

All power rails reach nominal within 20ms

- 1=> +3V_GPU
- 2=> +VGPU_CORE/+1V_GPU
- 3=> +VGPU_CORE PWRGD to enable +1.5V_GPU
- 4=> +1V_GPU PWRGD to enable +1.8V_GPU

NOTE

- 1.+3V to turn on +3V_GPU
- 2.+3V_GPU ready to enable +VGPU_CORE/+1V_GPU (+1V_GPU will ramp up before +VGPU_CORE)
- 3.+VGPU_CORE PWRGD to enable +1.5V_GPU
- 3.+1V_GPU PWRGD to enable +1.8V_GPU

TRAVIS_L ANX3110 power on sequence

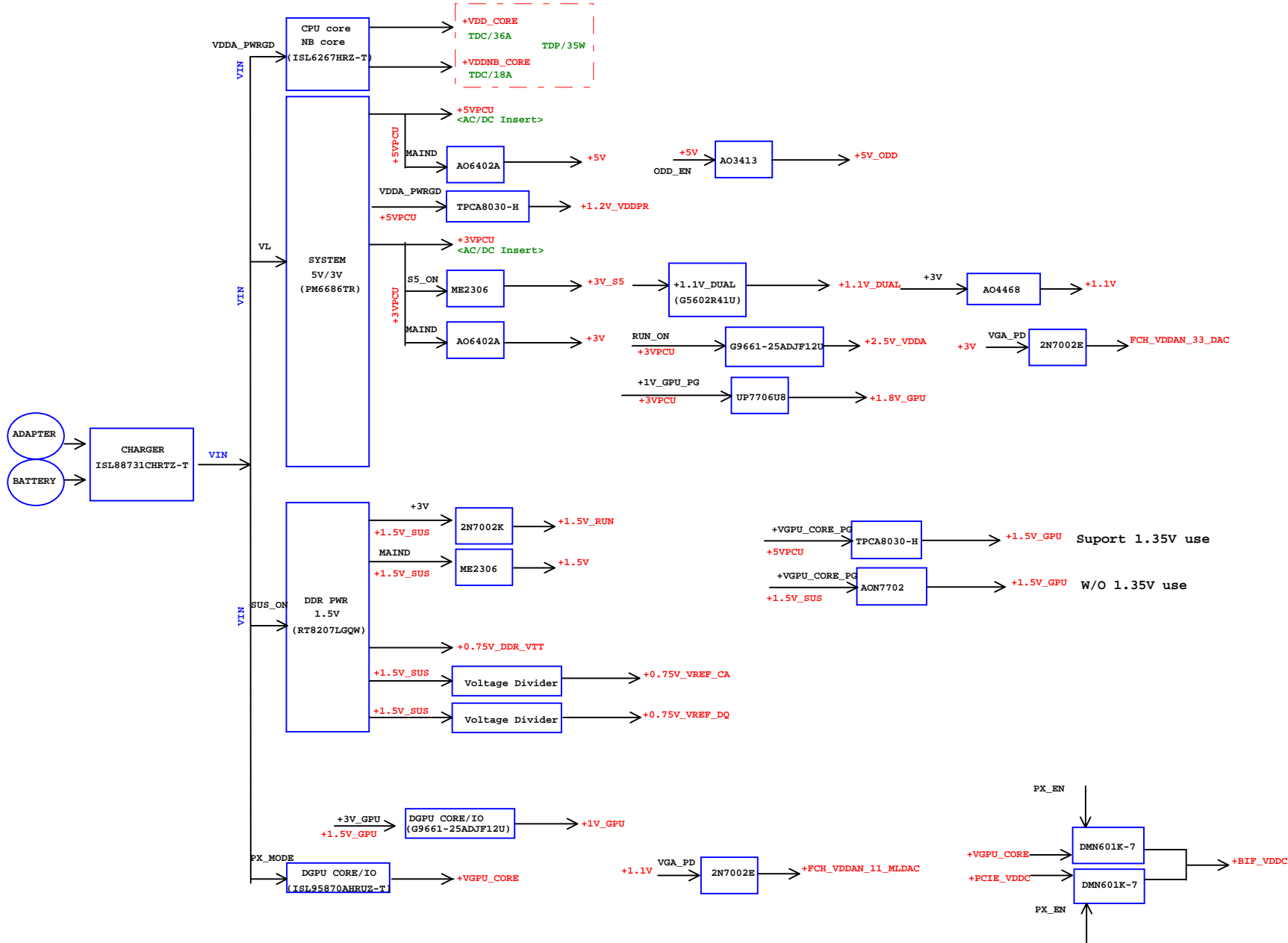
- 1.+3V must lead +1.2V_TRAVIS

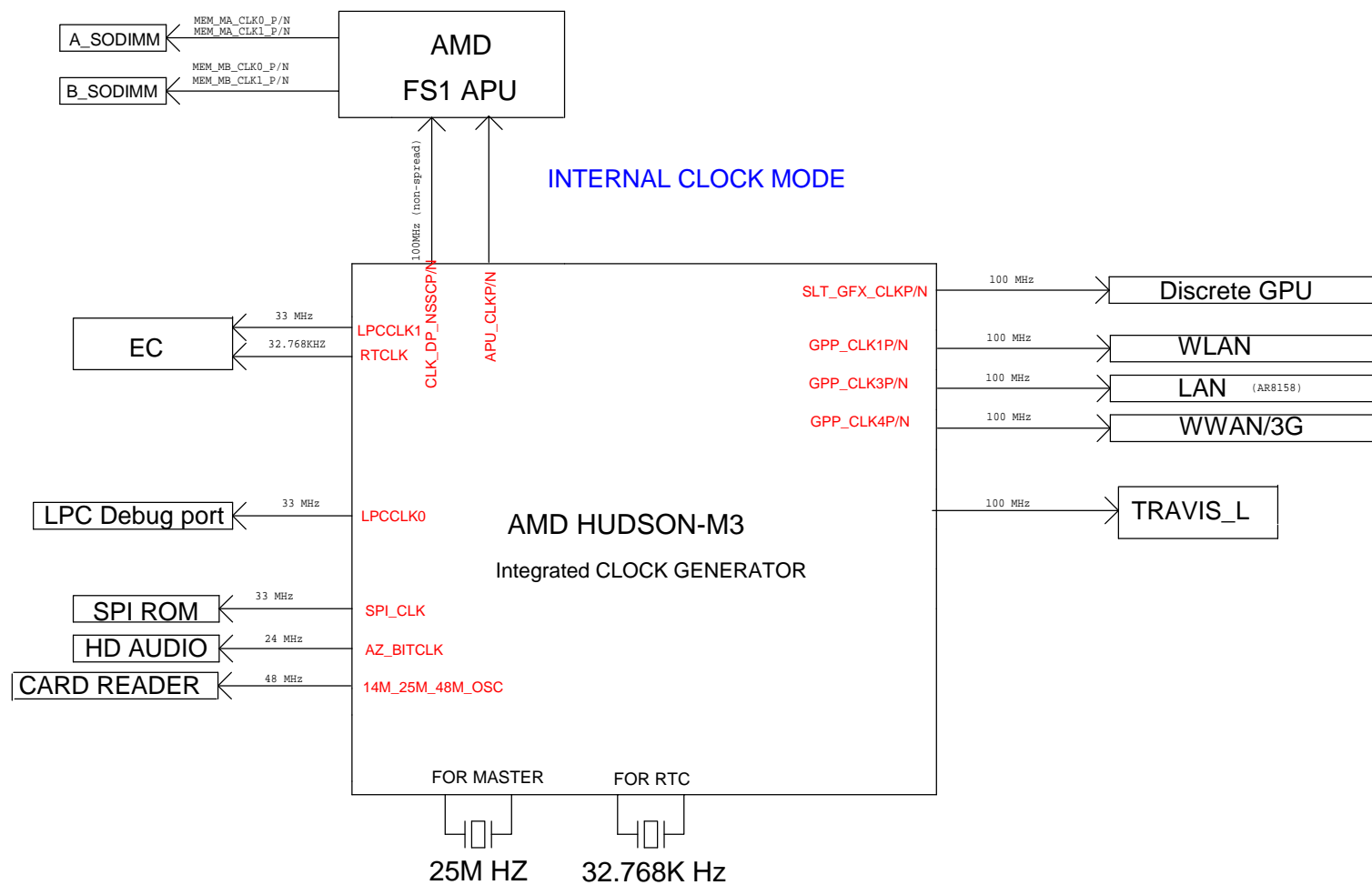
- 2.+1.2V_TRAVIS must lead TRAVIS_RST#

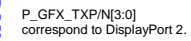
NOTE: FCH must output PCIE_RST#_TRAVIS or APU_PCIE_RST# after +1.2V_TRAVIS ready

APU GROUP A power


APU GROUP B power





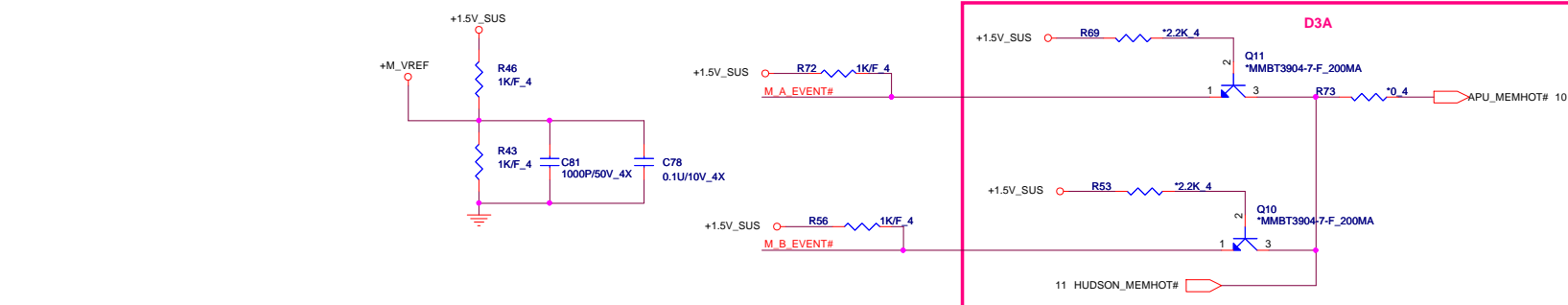


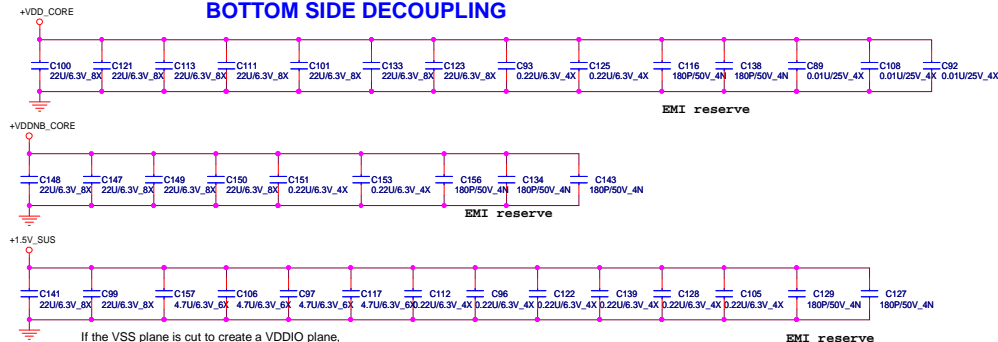
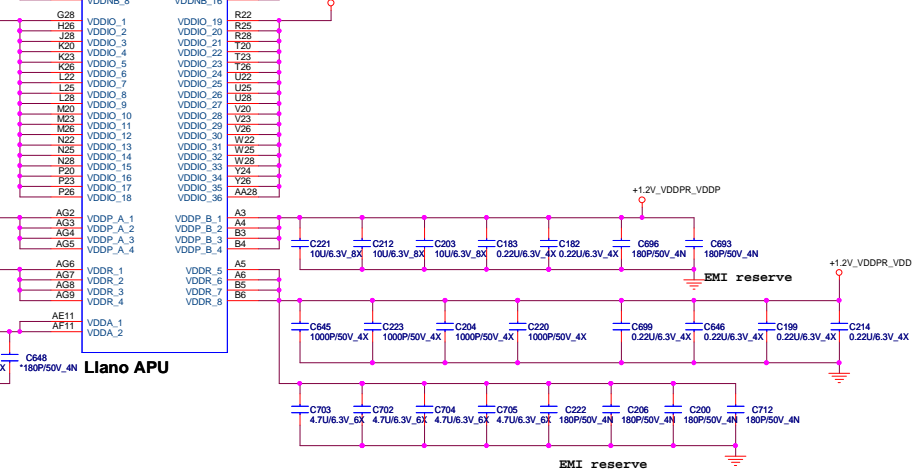
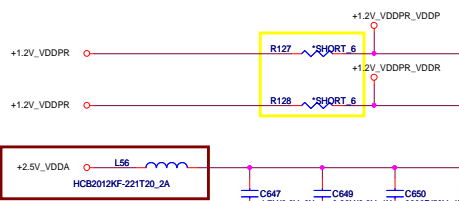
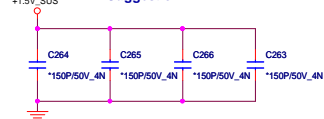
LAN
WLAN
3G

 Quanta Computer Inc. PROJECT : BLF_BLF		Rev 1C
Document Number	Llano PCIE/UMI/GPP	
Tuesday, April 19, 2011	Sheet 5 of 53	



Llano APU





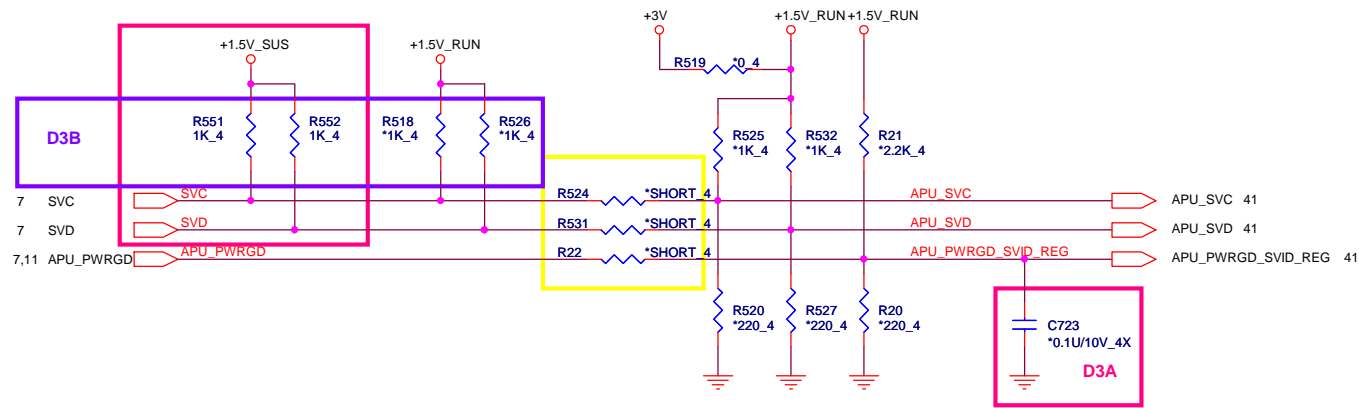
If the VSS plane is cut to create a VDDIO plane, ceramic capacitors are connected across the VDDIO and VSS plane split as follows

DECOUPLING between PROCESSOR and DIMMs

Across VDDIO and VSS split

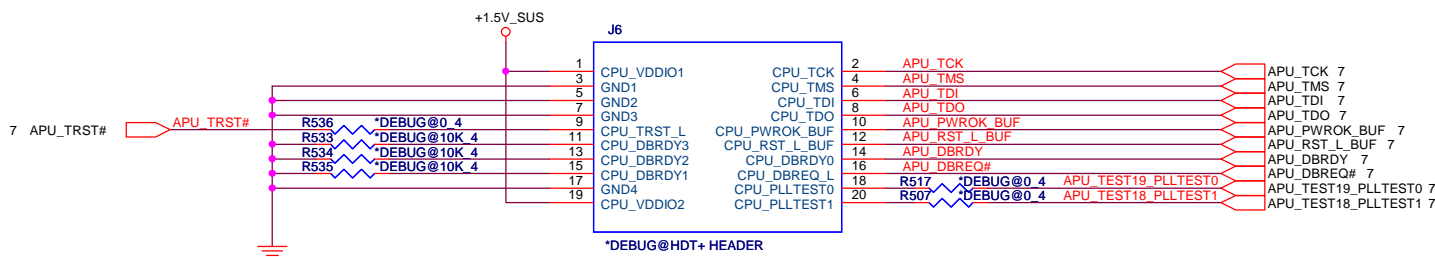



VID Override Circuit

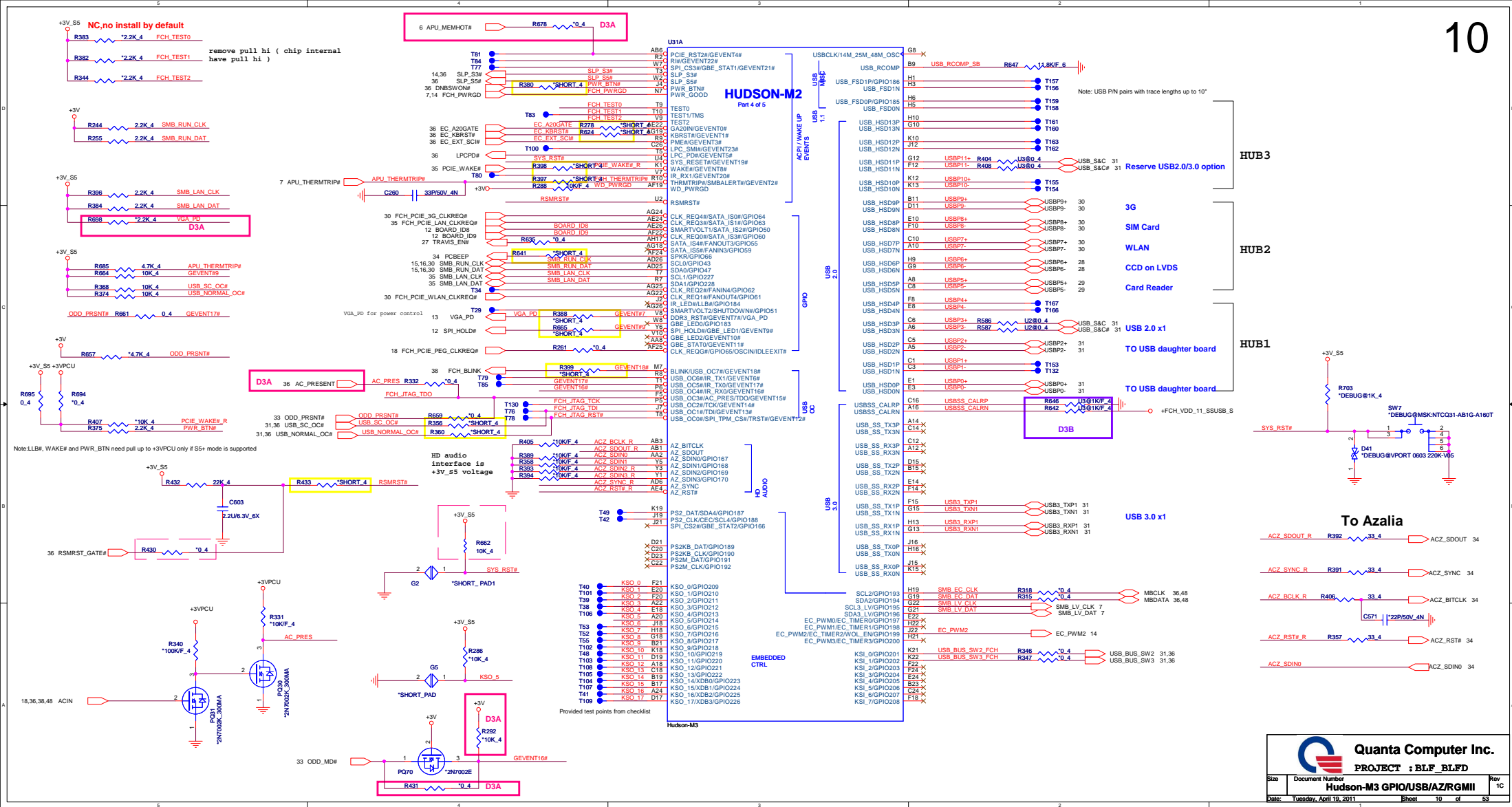


HDT+ Connector

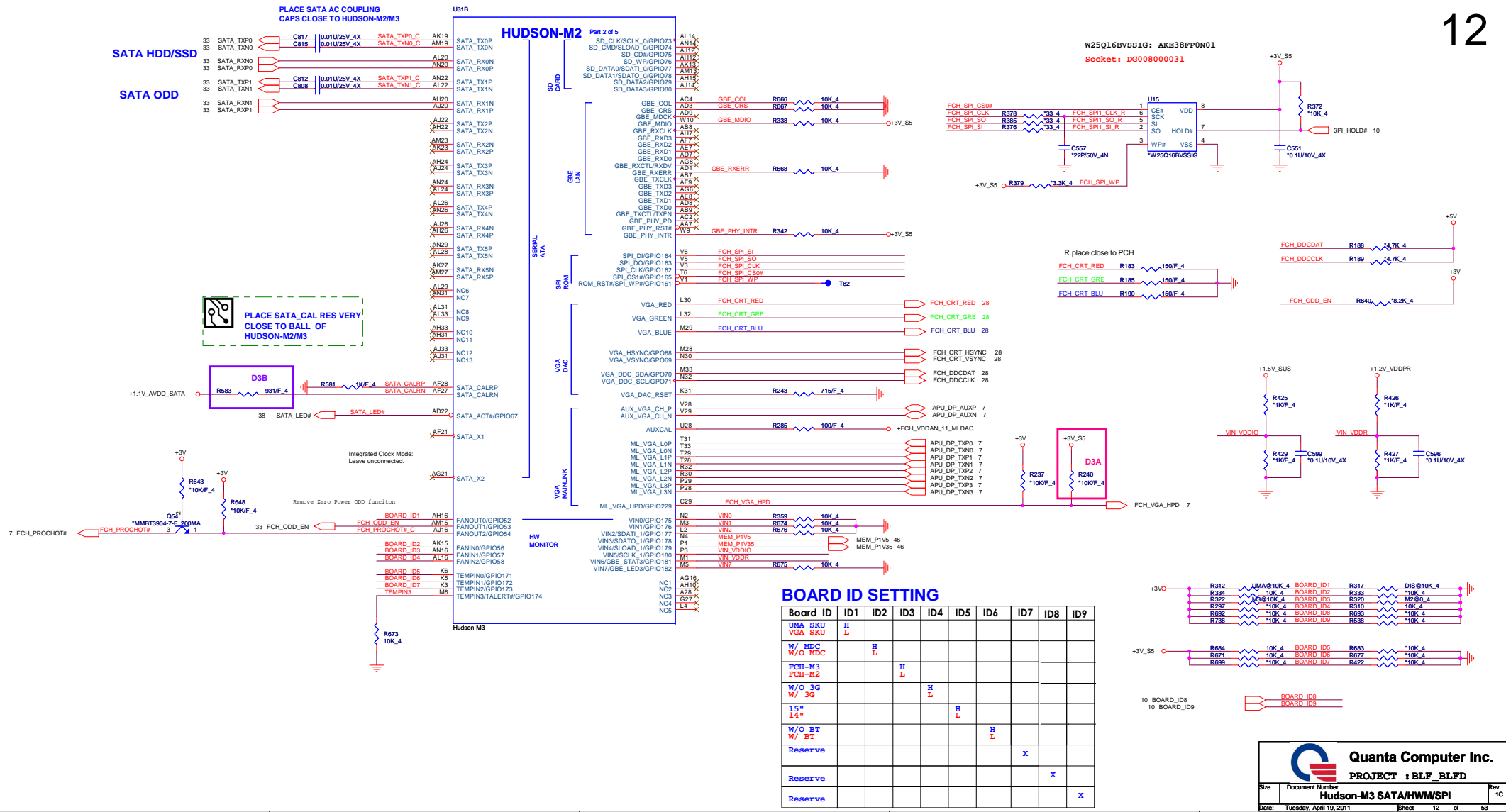
Debug only



 Quanta Computer Inc. PROJECT : BLF_BLF		Rev
		1C
Size	Document Number	
Llano DEBUG&OTHER		
Date:	Tuesday, April 19, 2011	Sheet 9 of 53









PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

VDD-- S/B CORE power

HUDSON-M2

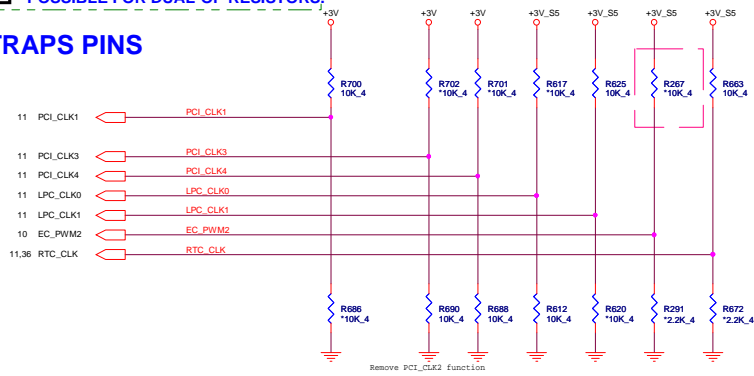
Part 5 of 5

A3	VSS.1	T25
A31	VSS.2	T27
B7	VSS.3	U6
B13	VSS.4	U14
D9	VSS.5	U17
D13	VSS.6	U20
E2	VSS.7	U21
E72	VSS.8	U22
F16	VSS.9	U23
F29	VSS.10	U24
F7	VSS.11	U25
F11	VSS.12	U26
F13	VSS.13	U27
F14	VSS.14	U28
F17	VSS.15	U29
F18	VSS.16	U30
F19	VSS.17	U31
F20	VSS.18	U32
F21	VSS.19	U33
F22	VSS.20	U34
F23	VSS.21	U35
F24	VSS.22	U36
F25	VSS.23	U37
F26	VSS.24	U38
F27	VSS.25	U39
F28	VSS.26	U40
F29	VSS.27	U41
F30	VSS.28	U42
F31	VSS.29	U43
F32	VSS.30	U44
F33	VSS.31	U45
F34	VSS.32	U46
F35	VSS.33	U47
F36	VSS.34	U48
F37	VSS.35	U49
F38	VSS.36	U50
F39	VSS.37	U51
F40	VSS.38	U52
F41	VSS.39	U53
F42	VSS.40	U54
F43	VSS.41	U55
F44	VSS.42	U56
F45	VSS.43	U57
F46	VSS.44	U58
F47	VSS.45	U59
F48	VSS.46	U60
F49	VSS.47	U61
F50	VSS.48	U62
F51	VSS.49	U63
F52	VSS.50	U64
F53	VSS.51	U65
F54	VSS.52	U66
F55	VSS.53	U67
F56	VSS.54	U68
F57	VSS.55	U69
F58	VSS.56	U70
F59	VSS.57	U71
F60	VSS.58	U72
F61	VSS.59	U73
F62	VSS.60	U74
F63	VSS.61	U75
F64	VSS.62	U76
F65	VSS.63	U77
F66	VSS.64	U78
F67	VSS.65	U79
F68	VSS.66	U80
F69	VSS.67	U81
F70	VSS.68	U82
F71	VSS.69	U83
F72	VSS.70	U84
F73	VSS.71	U85
F74	VSS.72	U86
F75	VSS.73	U87
F76	VSS.74	U88
F77	VSS.75	U89
F78	VSS.76	U90
F79	VSS.77	U91
F80	VSS.78	U92
F81	VSS.79	U93
F82	VSS.80	U94
F83	VSS.81	U95
F84	VSS.82	U96
F85	VSS.83	U97
F86	VSS.84	U98
F87	VSS.85	U99
F88	VSS.86	U100
F89	VSS.87	U101
F90	VSS.88	U102
F91	VSS.89	U103
F92	VSS.90	U104
F93	VSS.91	U105
F94	VSS.92	U106
F95	VSS.93	U107
F96	VSS.94	U108
F97	VSS.95	U109
F98	VSS.96	U110
F99	VSS.97	U111
F100	VSS.98	U112
F101	VSS.99	U113
F102	VSS.100	U114
F103	VSS.101	U115
F104	VSS.102	U116
F105	VSS.103	U117
F106	VSS.104	U118
F107	VSS.105	U119
F108	VSS.106	U120
F109	VSS.107	U121
F110	VSS.108	U122
F111	VSS.109	U123
F112	VSS.110	U124
F113	VSS.111	U125
F114	VSS.112	U126
F115	VSS.113	U127
F116	VSS.114	U128
F117	VSS.115	U129
F118	VSS.116	U130
F119	VSS.117	U131
F120	VSS.118	U132
F121	VSS.119	U133
F122	VSS.120	U134
F123	VSS.121	U135
F124	VSS.122	U136
F125	VSS.123	U137
F126	VSS.124	U138
F127	VSS.125	U139
F128	VSS.126	U140
F129	VSS.127	U141
F130	VSS.128	U142
F131	VSS.129	U143
F132	VSS.130	U144
F133	VSS.131	U145
F134	VSS.132	U146
F135	VSS.133	U147
F136	VSS.134	U148
F137	VSS.135	U149
F138	VSS.136	U150
F139	VSS.137	U151
F140	VSS.138	U152
F141	VSS.139	U153
F142	VSS.140	U154
F143	VSS.141	U155
F144	VSS.142	U156
F145	VSS.143	U157
F146	VSS.144	U158
F147	VSS.145	U159
F148	VSS.146	U160
F149	VSS.147	U161
F150	VSS.148	U162
F151	VSS.149	U163
F152	VSS.150	U164
F153	VSS.151	U165
F154	VSS.152	U166
F155	VSS.153	U167
F156	VSS.154	U168
F157	VSS.155	U169
F158	VSS.156	U170
F159	VSS.157	U171
F160	VSS.158	U172
F161	VSS.159	U173
F162	VSS.160	U174
F163	VSS.161	U175
F164	VSS.162	U176
F165	VSS.163	U177
F166	VSS.164	U178
F167	VSS.165	U179
F168	VSS.166	U180
F169	VSS.167	U181
F170	VSS.168	U182
F171	VSS.169	U183
F172	VSS.170	U184
F173	VSS.171	U185
F174	VSS.172	U186
F175	VSS.173	U187
F176	VSS.174	U188
F177	VSS.175	U189
F178	VSS.176	U190
F179	VSS.177	U191
F180	VSS.178	U192
F181	VSS.179	U193
F182	VSS.180	U194
F183	VSS.181	U195
F184	VSS.182	U196
F185	VSS.183	U197
F186	VSS.184	U198
F187	VSS.185	U199
F188	VSS.186	U200
F189	VSS.187	U201
F190	VSS.188	U202
F191	VSS.189	U203
F192	VSS.190	U204
F193	VSS.191	U205
F194	VSS.192	U206
F195	VSS.193	U207
F196	VSS.194	U208
F197	VSS.195	U209
F198	VSS.196	U210
F199	VSS.197	U211
F200	VSS.198	U212
F201	VSS.199	U213
F202	VSS.200	U214
F203	VSS.201	U215
F204	VSS.202	U216
F205	VSS.203	U217
F206	VSS.204	U218
F207	VSS.205	U219
F208	VSS.206	U220
F209	VSS.207	U221
F210	VSS.208	U222
F211	VSS.209	U223
F212	VSS.210	U224
F213	VSS.211	U225
F214	VSS.212	U226
F215	VSS.213	U227
F216	VSS.214	U228
F217	VSS.215	U229
F218	VSS.216	U230
F219	VSS.217	U231
F220	VSS.218	U232
F221	VSS.219	U233
F222	VSS.220	U234
F223	VSS.221	U235
F224	VSS.222	U236
F225	VSS.223	U237
F226	VSS.224	U238
F227	VSS.225	U239
F228	VSS.226	U240
F229	VSS.227	U241
F230	VSS.228	U242
F231	VSS.229	U243
F232	VSS.230	U244
F233	VSS.231	U245
F234	VSS.232	U246
F235	VSS.233	U247
F236	VSS.234	U248
F237	VSS.235	U249
F238	VSS.236	U250
F239	VSS.237	U251
F240	VSS.238	U252
F241	VSS.239	U253
F242	VSS.240	U254
F243	VSS.241	U255
F244	VSS.242	U256
F245	VSS.243	U257
F246	VSS.244	U258
F247	VSS.245	U259
F248	VSS.246	U260
F249	VSS.247	U261
F250	VSS.248	U262
F251	VSS.249	U263
F252	VSS.250	U264
F253	VSS.251	U265
F254	VSS.252	U266
F255	VSS.253	U267
F256	VSS.254	U268
F257	VSS.255	U269
F258	VSS.256	U270
F259	VSS.257	U271
F260	VSS.258	U272
F261	VSS.259	U273
F262	VSS.260	U274
F263	VSS.261	U275
F264	VSS.262	U276
F265	VSS.263	U277
F266	VSS.264	U278
F267	VSS.265	U279
F268	VSS.266	U280
F269	VSS.267	U281
F270	VSS.268	U282
F271	VSS.269	U283
F272	VSS.270	U284
F273	VSS.271	U285
F274	VSS.272	U286
F275	VSS.273	U287
F276	VSS.274	U288
F277	VSS.275	U289
F278	VSS.276	U290
F279	VSS.277	U291
F280	VSS.278	U292
F281	VSS.279	U293
F282	VSS.280	U294
F283	VSS.281	U295
F284	VSS.282	U296
F285	VSS.283	U297
F286	VSS.284	U298
F287	VSS.285	U299
F288	VSS.286	U300
F289	VSS.287	U301
F290	VSS.288	U302
F291	VSS.289	U303
F292	VSS.290	U304
F293	VSS.291	U305
F294	VSS.292	U306
F295	VSS.293	U307
F296	VSS.294	U308
F297	VSS.295	U309
F298	VSS.296	U310
F299	VSS.297	U311
F300	VSS.298	U312
F301	VSS.299	U313
F302	VSS.300	U314
F303	VSS.301	U315
F304	VSS.302	U316
F305	VSS.303	U317
F306	VSS.304	U318
F307	VSS.305	U319
F308	VSS.306	U320
F309	VSS.307	U321
F310	VSS.308	U322
F311	VSS.309	U323
F312	VSS.310	U324
F313	VSS.311	U325
F314	VSS.312	U326
F315	VSS.313	U327
F316	VSS.314	U328
F317	VSS.315	U329
F318	VSS.316	U330
F319	VSS.317	U331
F320	VSS.318	U332
F321	VSS.319	U333
F322	VSS.320	U334
F323	VSS.321	U335
F324	VSS.322	U336
F325	VSS.323	U337
F326	VSS.324	U338
F327	VSS.325	U339
F328	VSS.326	U340
F329	VSS.327	U341
F330	VSS.328	U342
F331	VSS.329	U343
F332	VSS.330	U344
F333	VSS.331	U345
F334	VSS.332	U346
F335	VSS.333	U347
F336	VSS.334	U348
F337	VSS.335	U349
F338	VSS.336	U350
F339	VSS.337	U351
F340	VSS.338	U352
F341	VSS.339	U353
F342	VSS.340	U354
F343	VSS.341	U355
F344	VSS.342	U356
F345	VSS.343	U357
F346	VSS.344	U358
F347	VSS.345	U359
F348	VSS.346	U360
F349	VSS.347	U361
F350	VSS.348	U362
F351	VSS.349	U363
F352	VSS.350	U364
F353	VSS.351	U365
F354	VSS.352	U366
F355	VSS.353	U367
F356	VSS.354	U368
F357	VSS.355	U369
F358	VSS.356	U370
F359	VSS.357	U371
F360	VSS.358	U372
F361	VSS.359	U373
F362	VSS.360	U374
F363	VSS.361	U375
F364	VSS.362	U376
F365	VSS.363	U377
F366	VSS.364	U378
F367	VSS.365	U379
F368	VSS.366	U380
F369	VSS.367	U381
F370	VSS.368	U382
F371	VSS.369	U383
F372	VSS.370	U384
F373	VSS.371	U385
F374	VSS.372	U386
F375	VSS.373	U387
F376	VSS.374	U388
F377	VSS.375	U389
F378	VSS.376	U390
F379	VSS.377	U



OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

STRAPS PINS

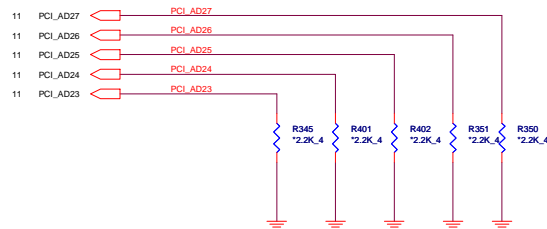


REQUIRED STRAPS

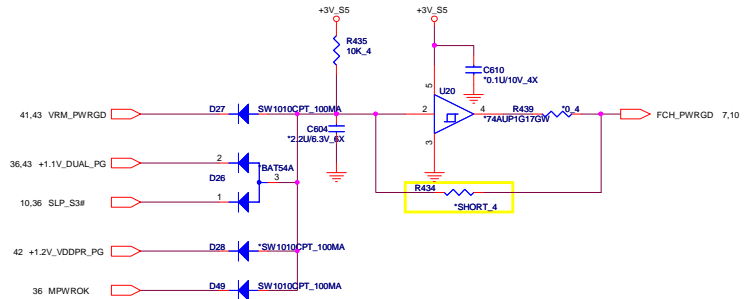
		PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	*****	ALLOW PCIe Gen2 DEFAULT	*****	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	*****	FORCE PCIe Gen1	*****	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM	S5 PLUS MODE ENABLED

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]



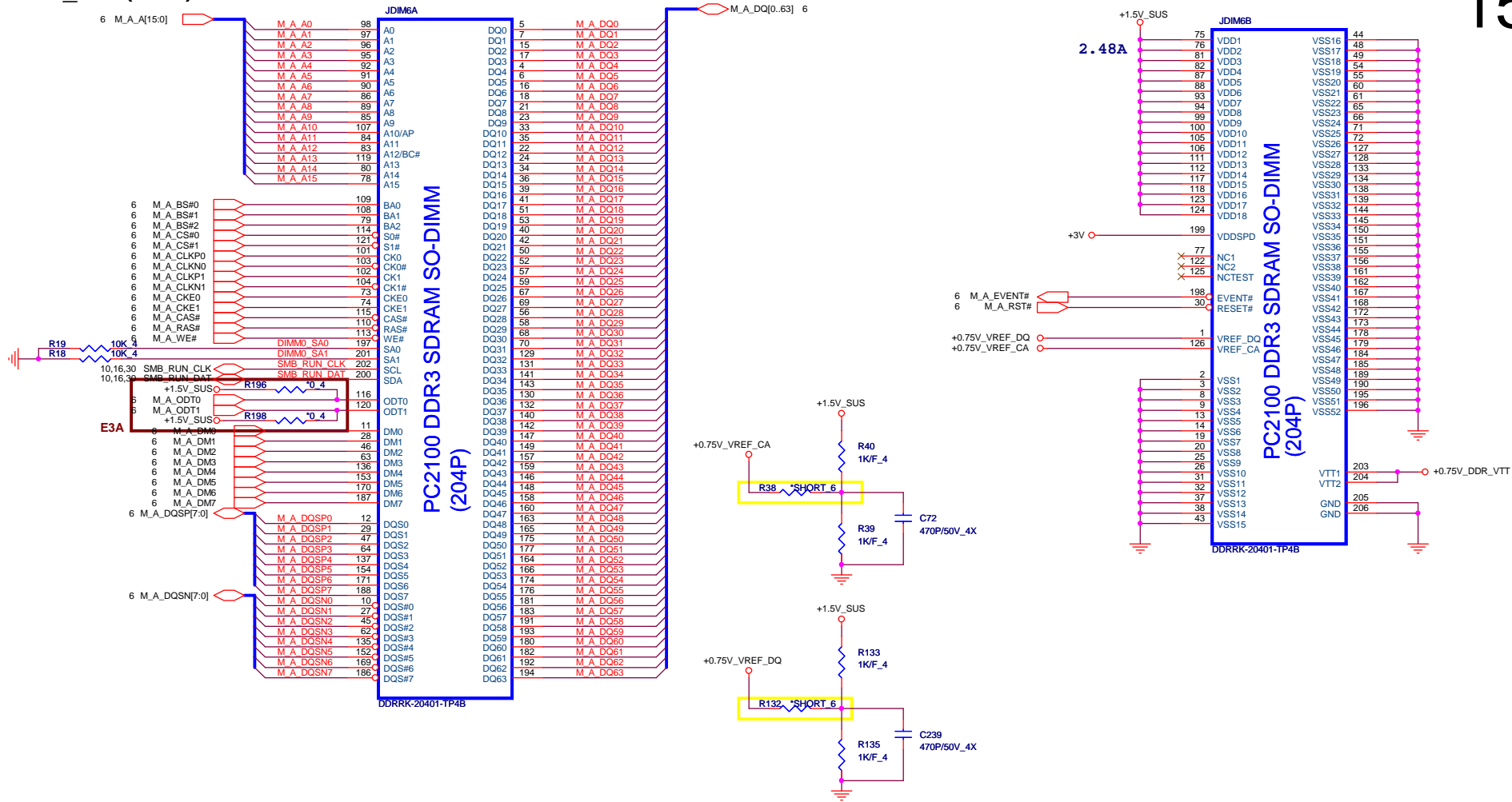
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIe STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIe STRAPS	ENABLE PCI MEM BOOT



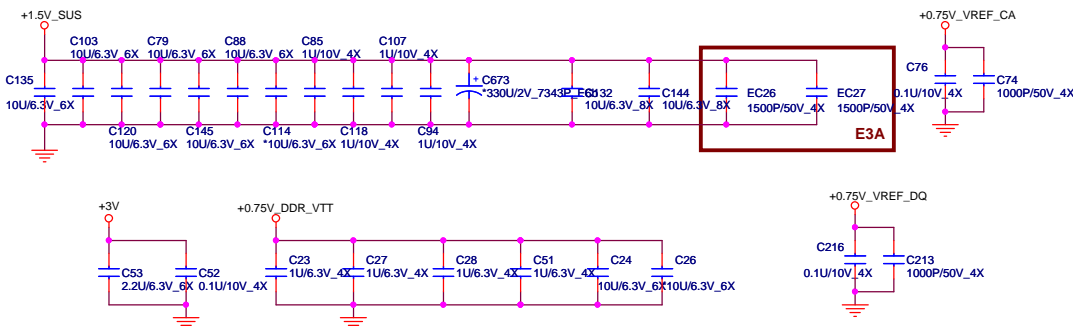
FCH PWRGD CKT

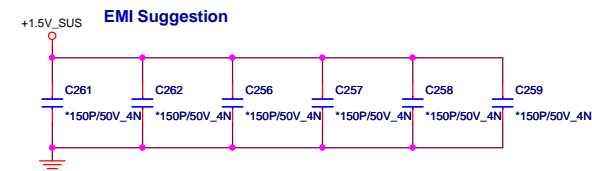
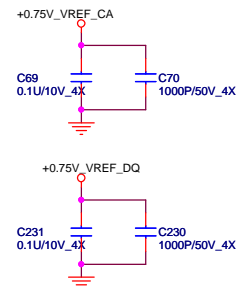
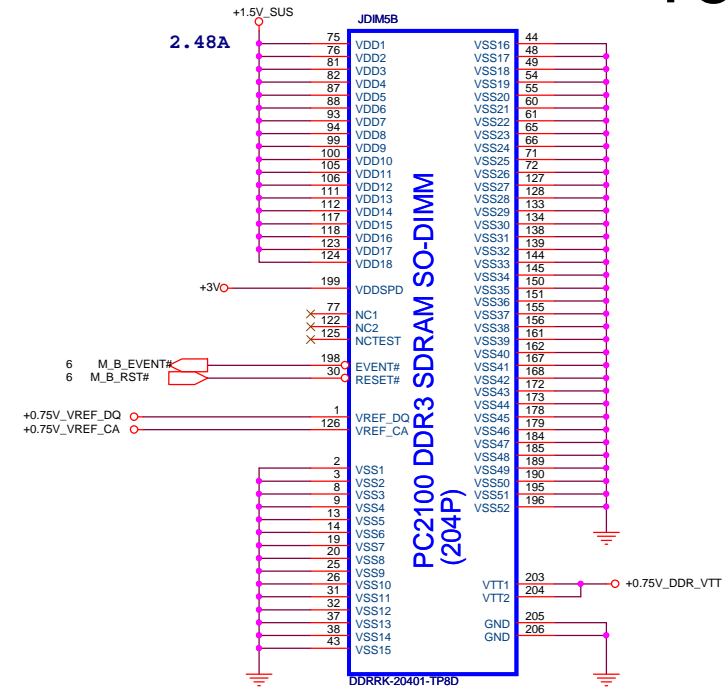
DDR STD (DDR)

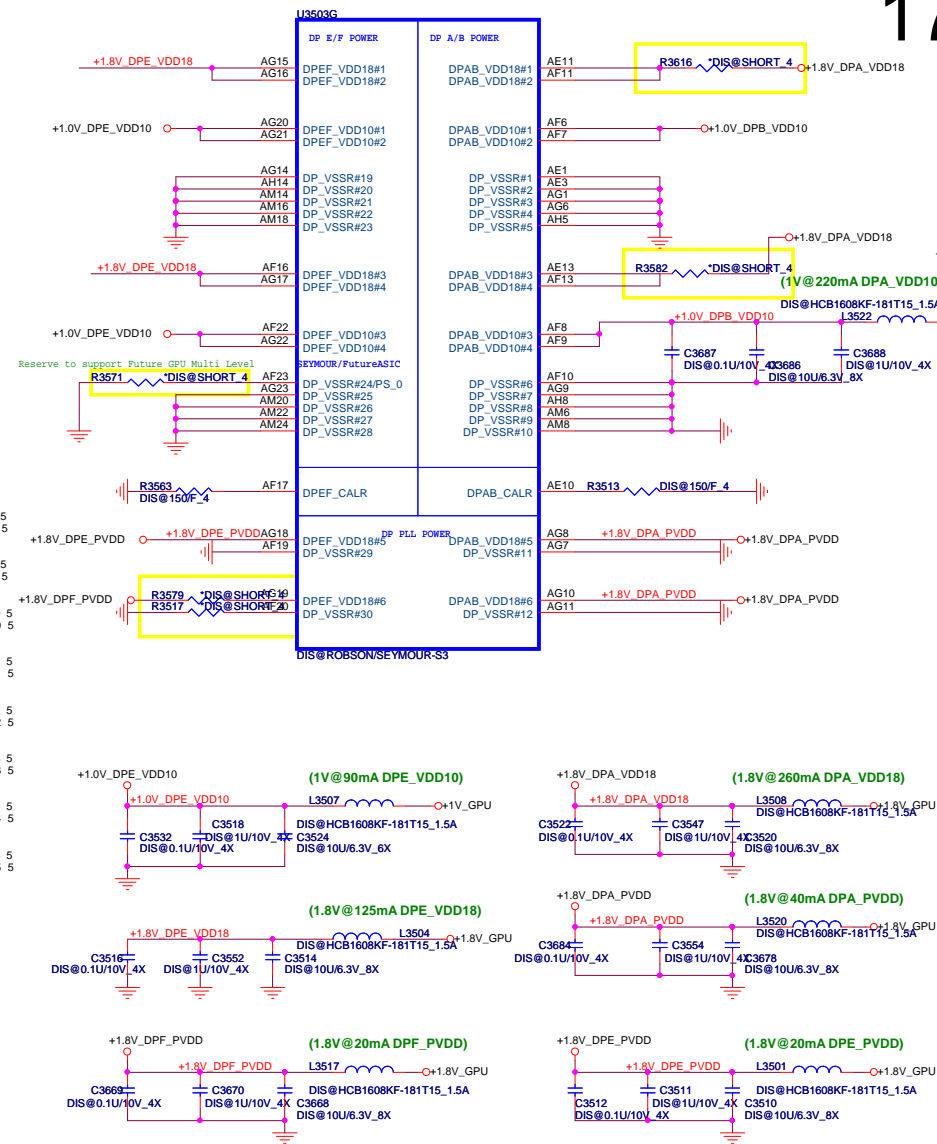
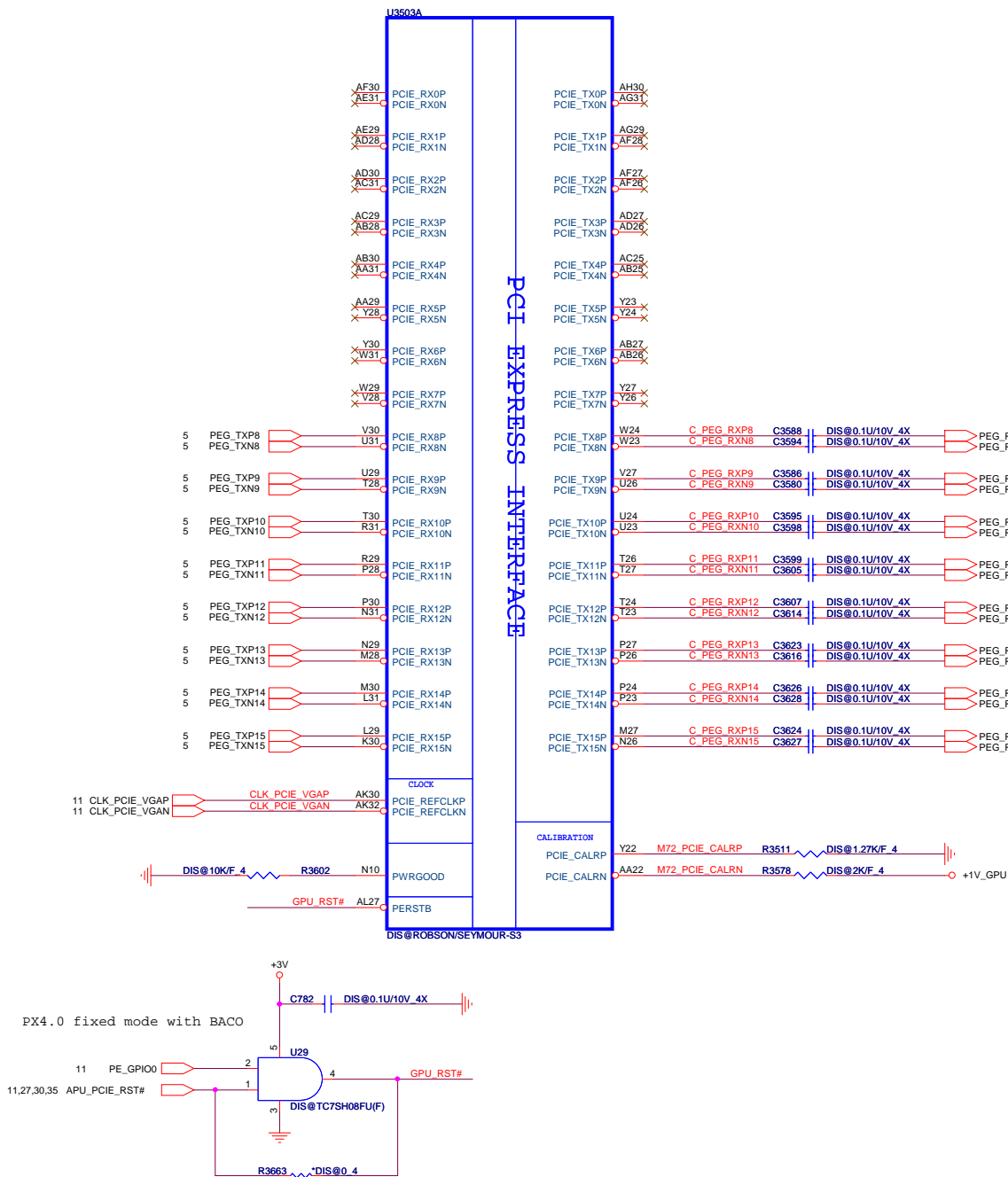
15



Place these Caps near SoDimm0.










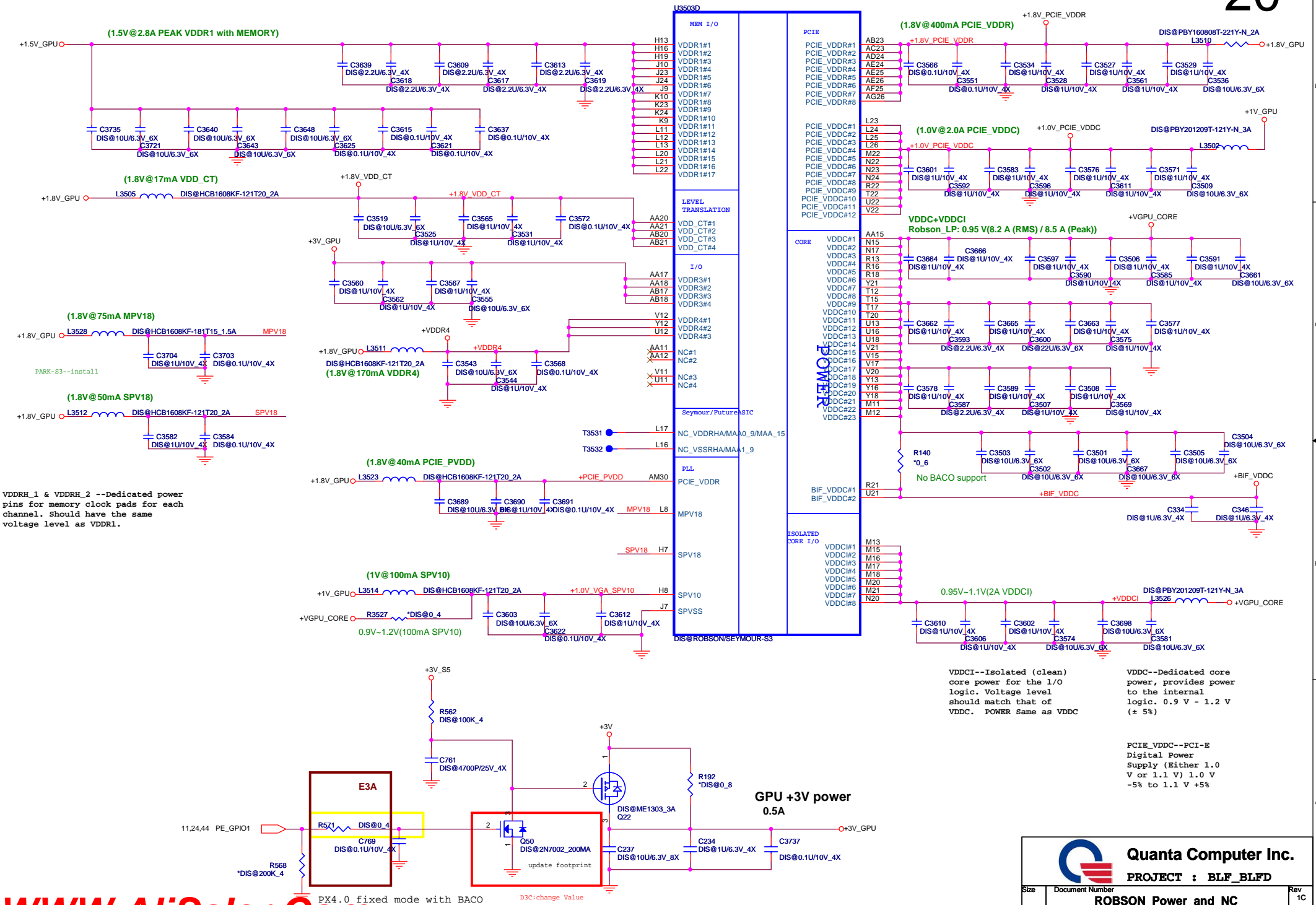


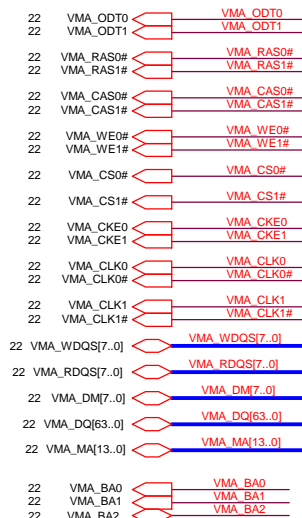
<p>AMD RESERVED CONFIGURATION STRAPS</p> <p>ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET</p>	
H2SYNC	GENERICC
<p>PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET</p>	
GPIO21_BB_EN	

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

Timing diagram for GPIO signals. The diagram shows eight GPIO signals (GPIO0, GPIO1, GPIO2, SOUT_GPIO8, GENERICC, DAC2_VSY, DAC2_HSY, GPIO22, GPIO10_ROMSCK) connected to a +3V_GPI pin. Each signal is shown with a red trapezoidal pulse and a blue wavy line representing a signal transition. The signals are labeled with their respective pin numbers (R3585, R3580, R3581, R3584, R3514, R3562, R3572, R3529, R3650) and a timing constraint of *DIS@10K/F 4.

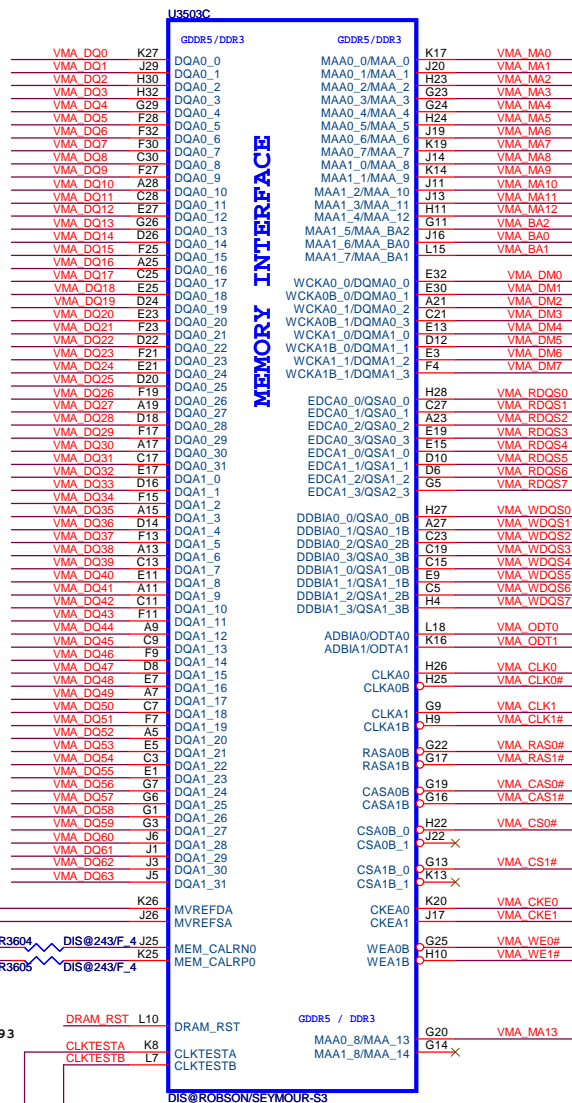
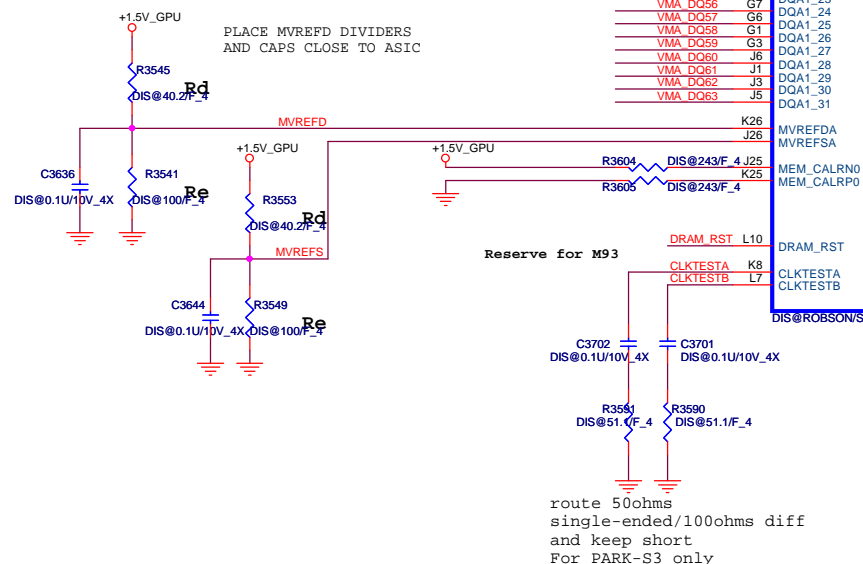
 Quanta Computer Inc. PROJECT : BLF_BLF		
Size	Document Number	Rev
	ROBSON_XT GND / LVDS/ Straps	1C
Date:	Tuesday, April 19, 2011	Sheet 19 of 53



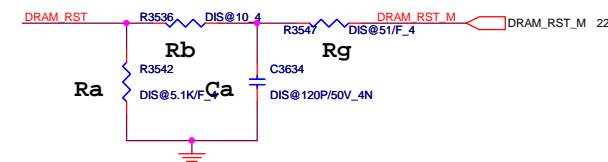


support 1gbt
VRAM (64M X 16)

DIVIDER RESISTORS	M93	PARK
MVREF TO 1.8V (Rd)	100R	40.2R
MVREF TO GND (Re)	100R	100R



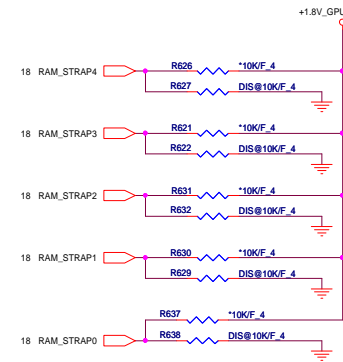
Designator	Robson
Ra	5K
Rb	10R
Ca	120pF
Rg	51R



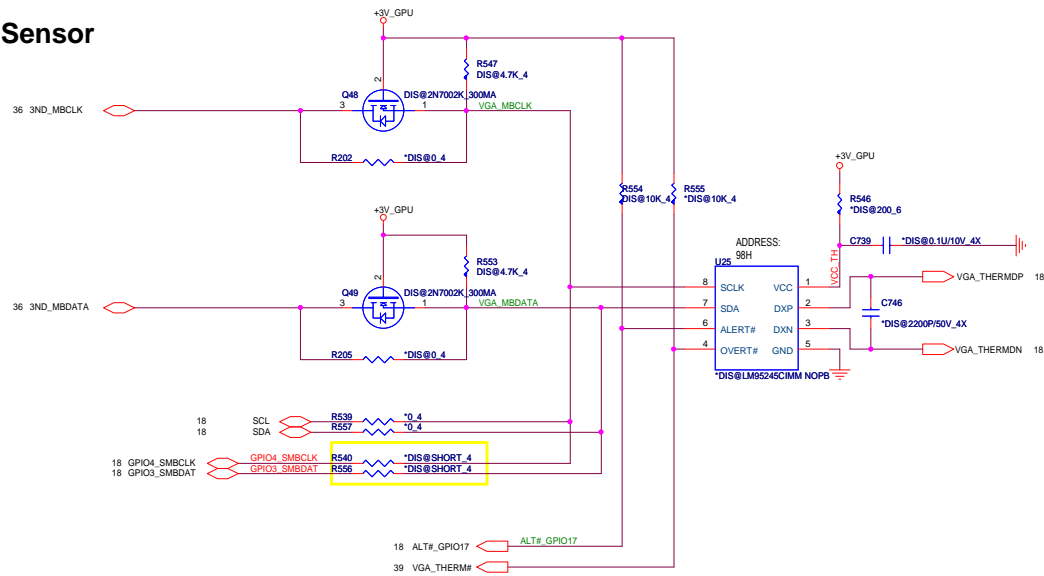


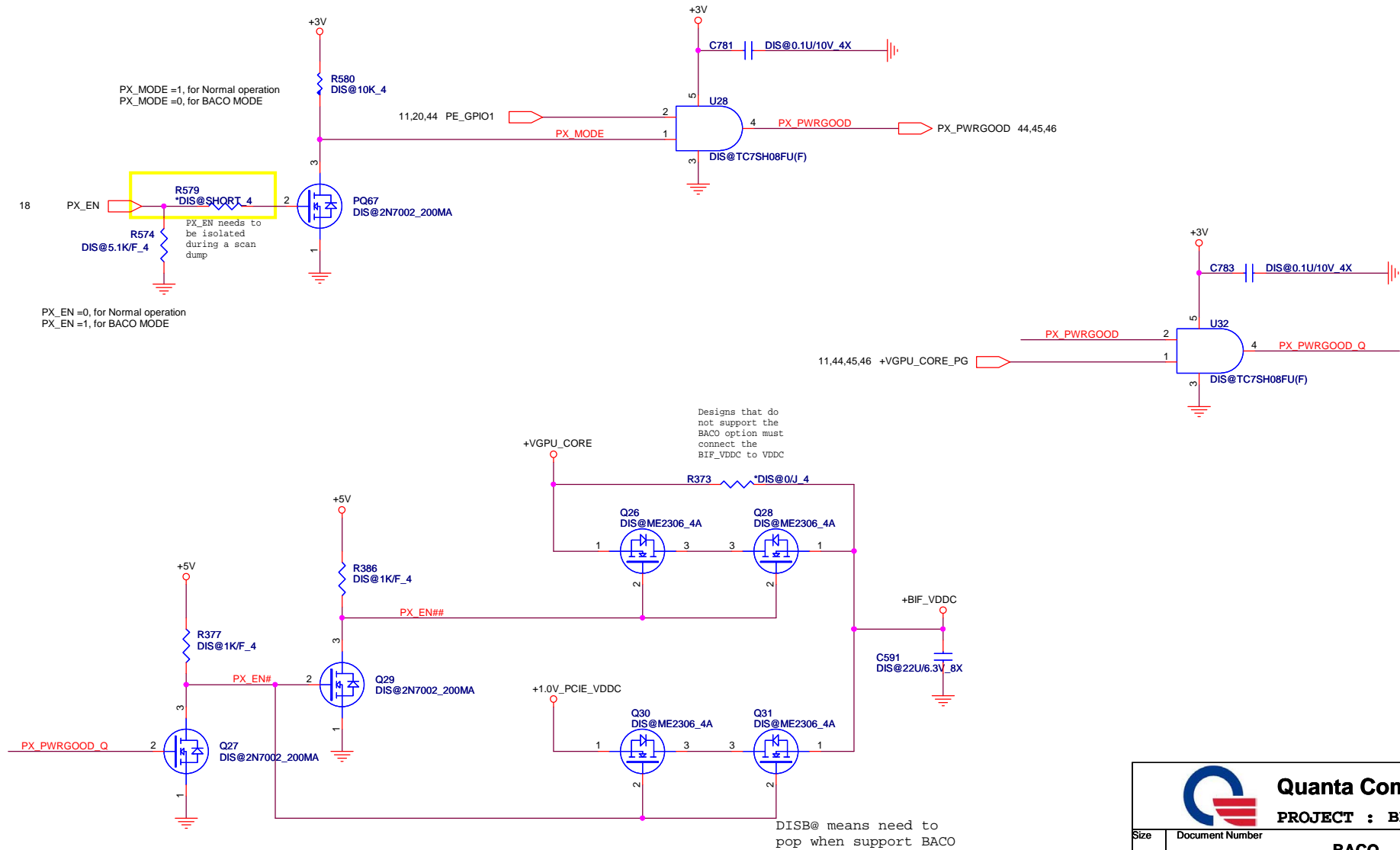
VRAM Memory TYPE


Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP3	RAM_STRAP2	RAM_STRAP1	RAM_STRAP0	RAM_STRAP4	
				DVPDATA_3	DVPDATA_2	DVPDATA_1	DVPDATA_0	15"	14"
Hynix	H5TQ1G63DFR-11C	AKD5LZWTW02 (64M*16-1Gb)	512MB	0	1	0	0	0	1
	H5TQ2G63BFR-11C	AKD5MGWTW00 (128M*16-2Gb)	1GB	0	0	0	0	0	1
Samsung	K4W1G1646G-BC11	AKD5EGGT500 (64M*16-1Gb)	512MB	0	1	0	1	0	1
	K4W2G1646C-HC11	AKD5MGWT500 (128M*16-2Gb)	1GB	0	0	0	1	0	1




Thermal Sensor





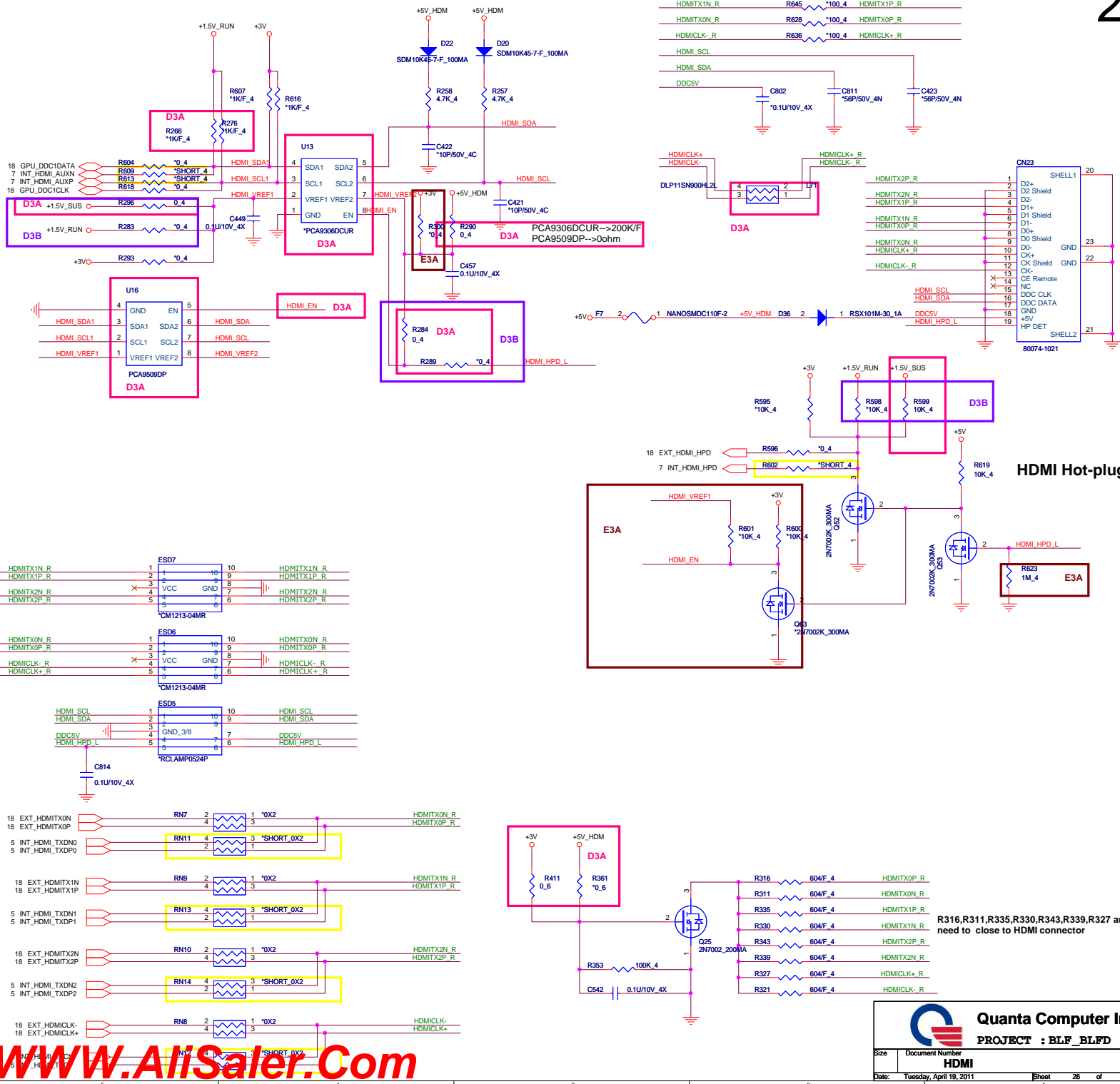
 Quanta Computer Inc. PROJECT : BLF_BLFD		Size	Document Number	Rev
				1C
Date: Tuesday, April 19, 2011		Sheet 24 of 53		



Quanta Computer Inc.

PROJECT : BLF_BLFD

Size	Document Number	Rev
	Blank	1C
Date:	Tuesday, April 19, 2011	Sheet 25 of 53

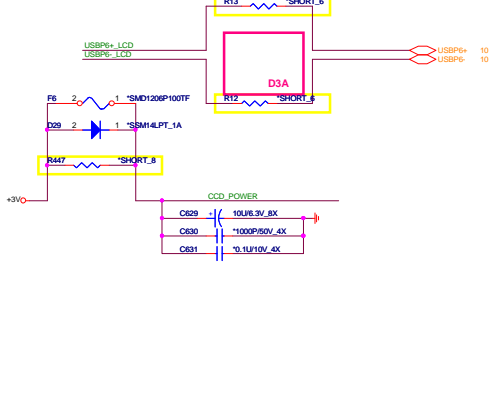


HDMI Hot-plug

R316,R311,R335,R330,R343,R339,R327 and R321 need to close to HDMI connector

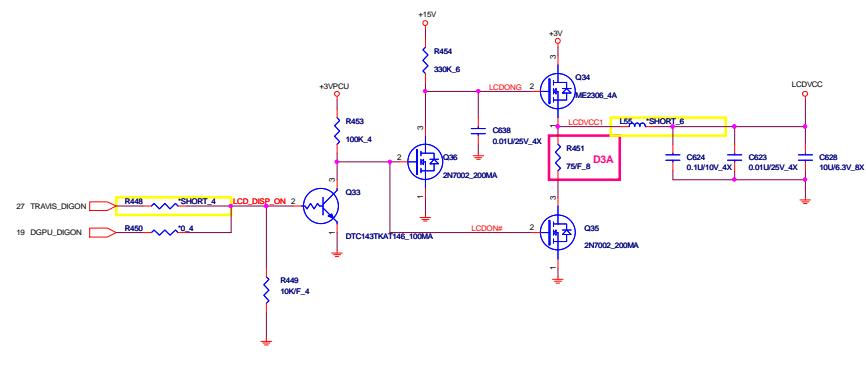


CCD [CCD]



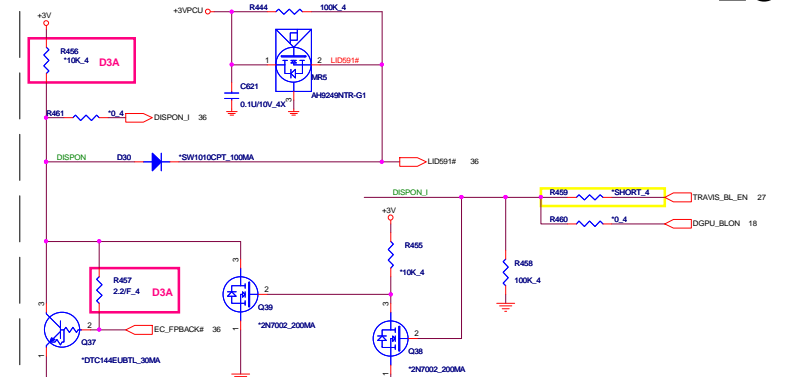
LCD POWER SWITCH

[LDS]



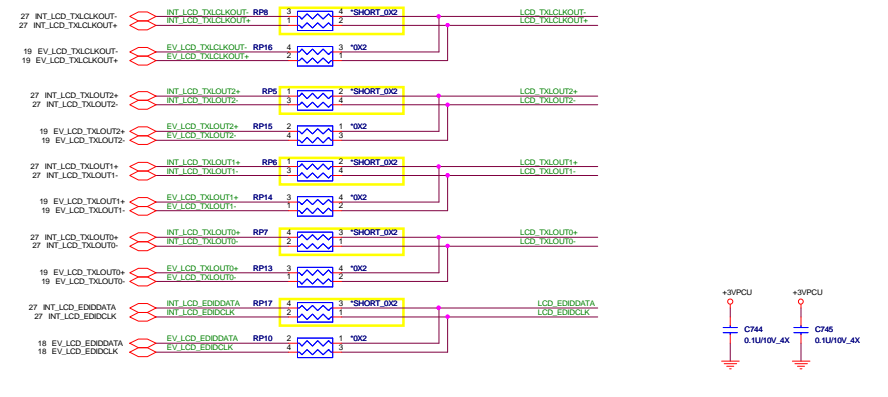
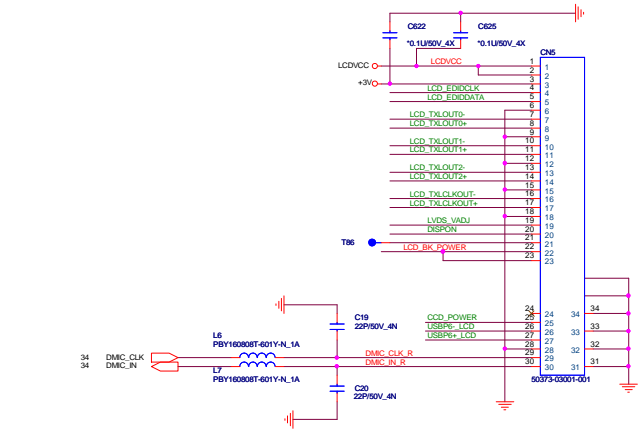
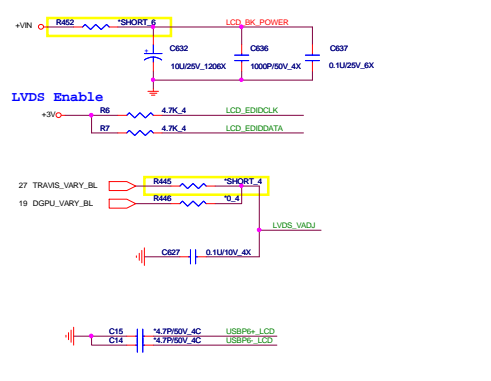
HALL SENSOR&BACK LIGHT SWITCH

[HSR]

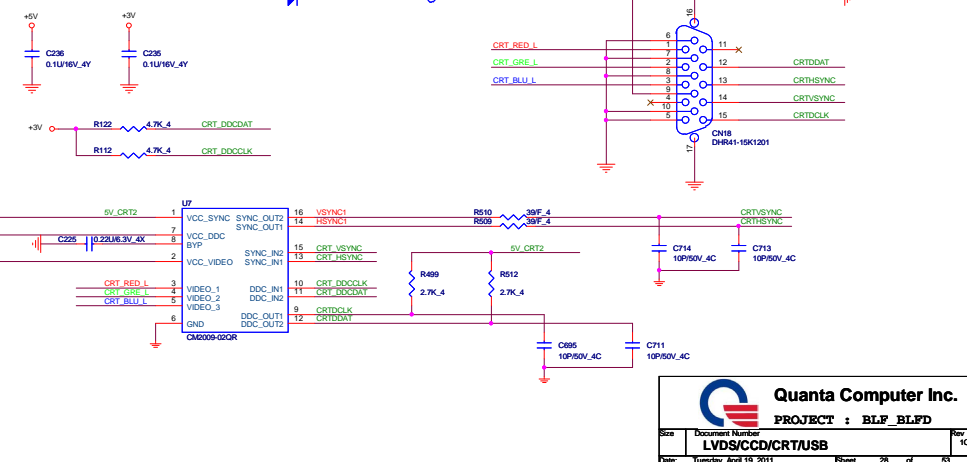
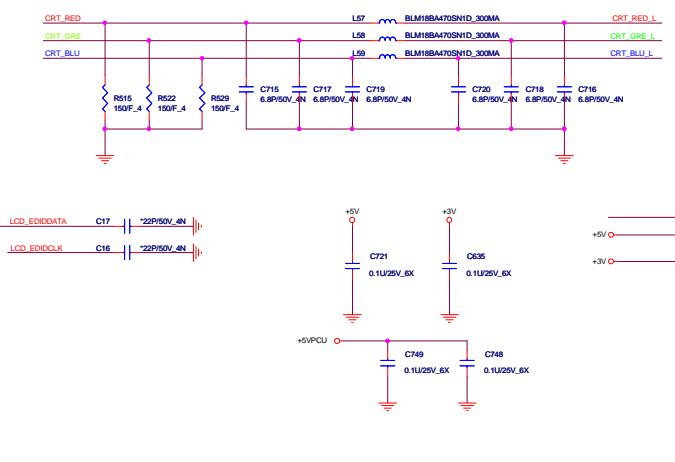
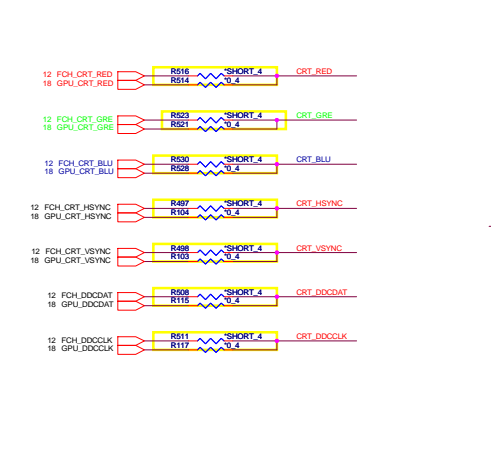


[LDS]

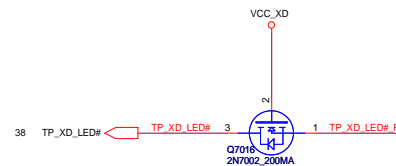
LCD Panel Module



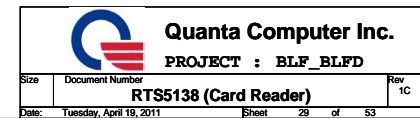
CRT [CRT]



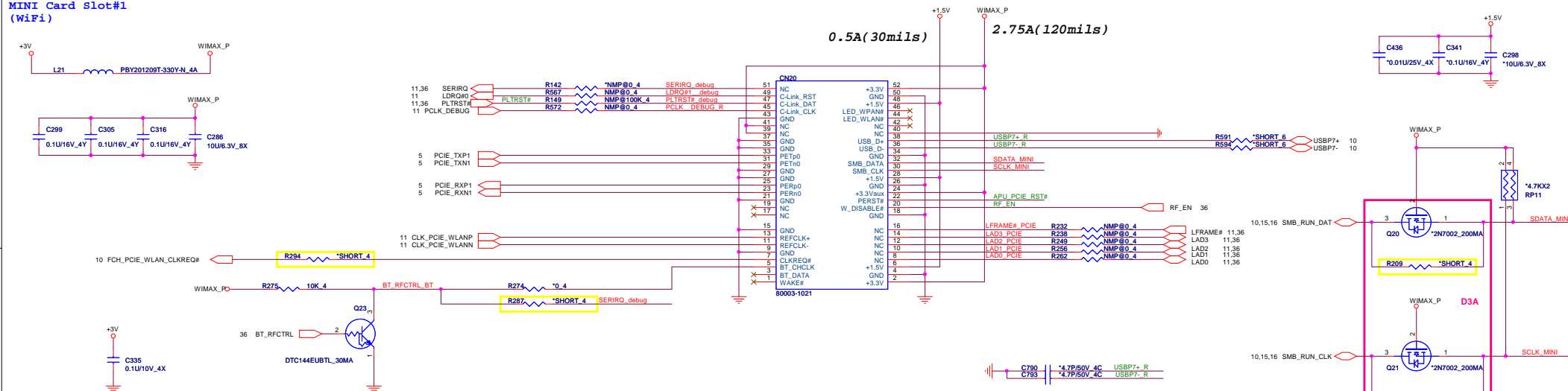
Card reader controller <MMC>



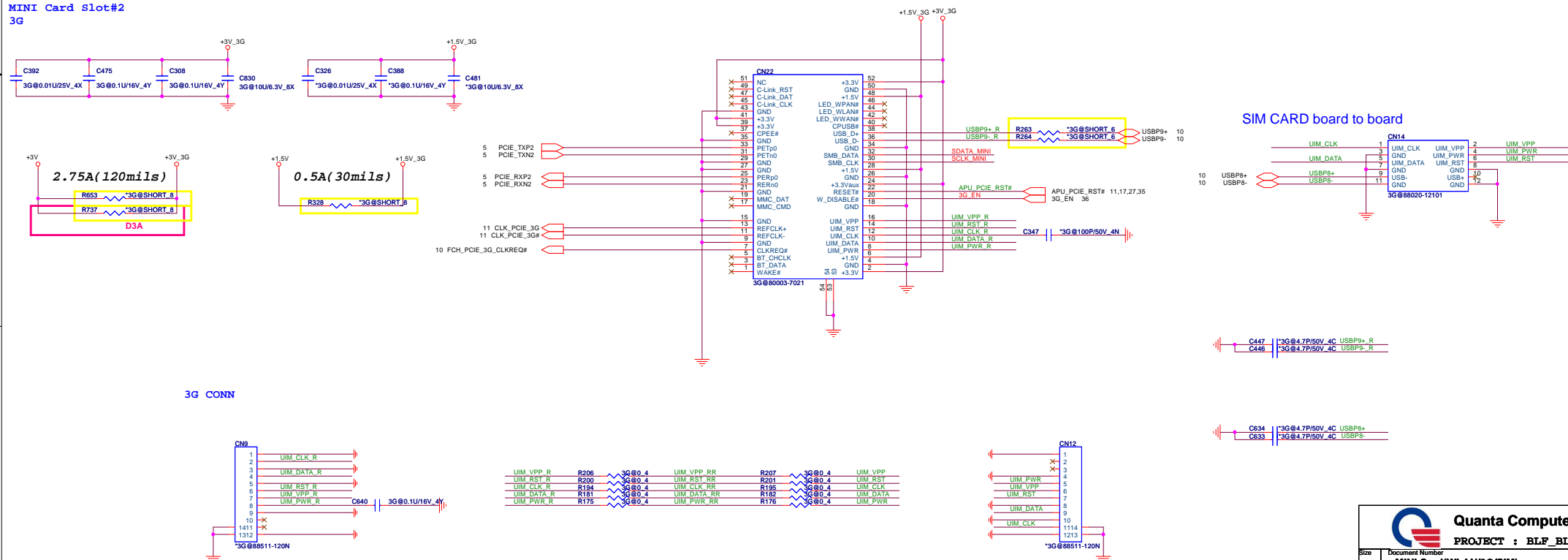
29



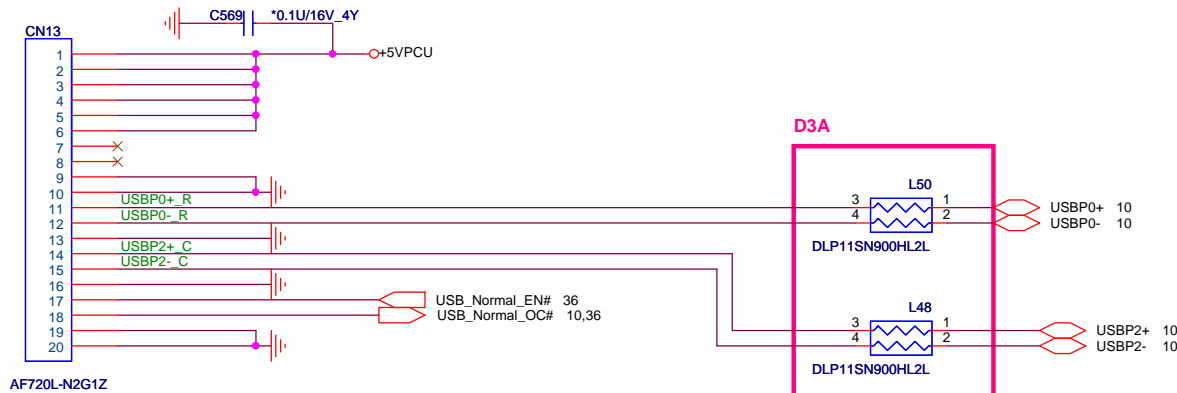
MINI Card Slot#1 (WiFi)



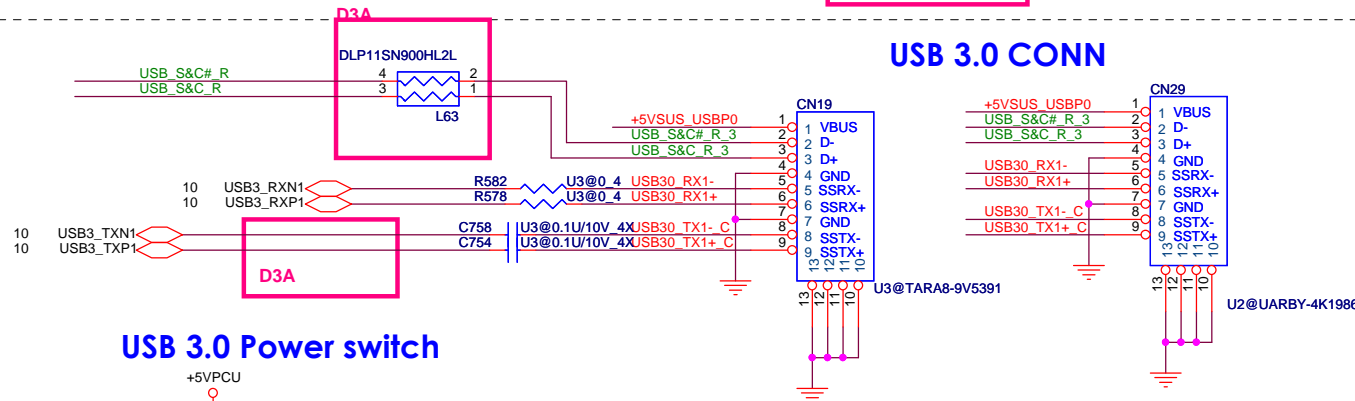
MINI Card Slot#2 3G



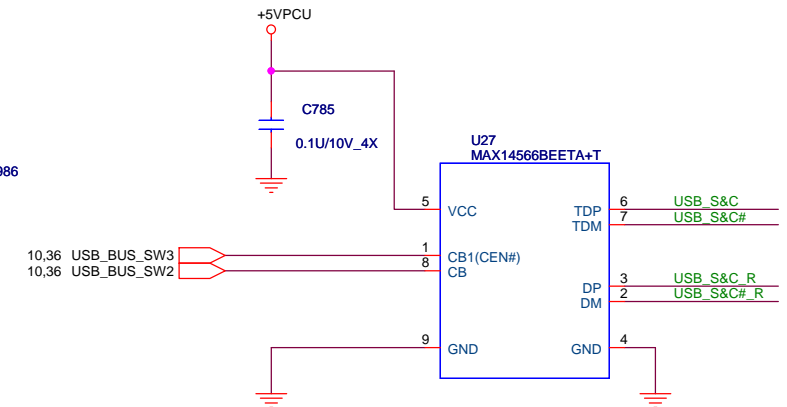
USB board



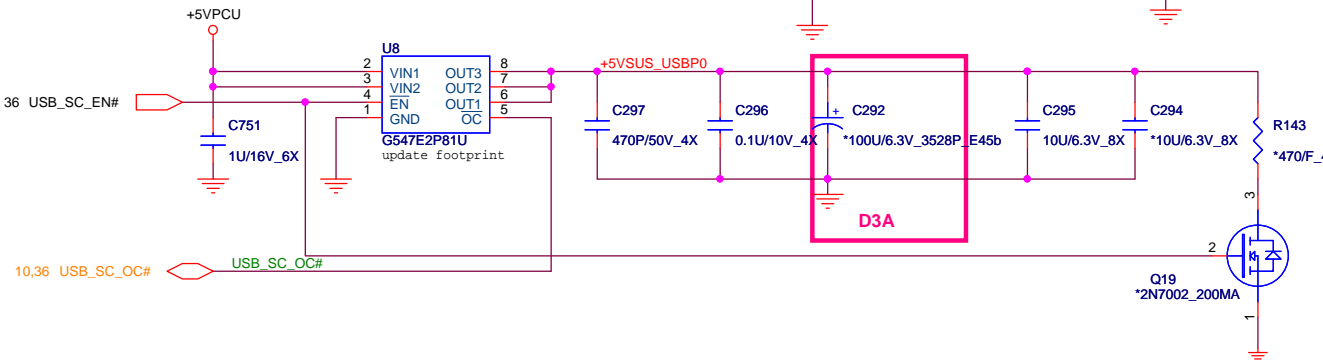
USB 3.0 CONN



USB Sleep & Charge MAXIM solution



USB 3.0 Power switch



CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	X	Pass-Through(USB) mode: Connect DP/DM to TDP/TDM

10 USB_S&C#
10 USB_S&C



Quanta Computer Inc.

PROJECT : BLF_BLFD

Size Document Number

USB2.0X1+USB3.0X1

Rev 1C

Date: Tuesday, April 19, 2011 Sheet 31 of 53

D

D

C

C

B

B

A

A



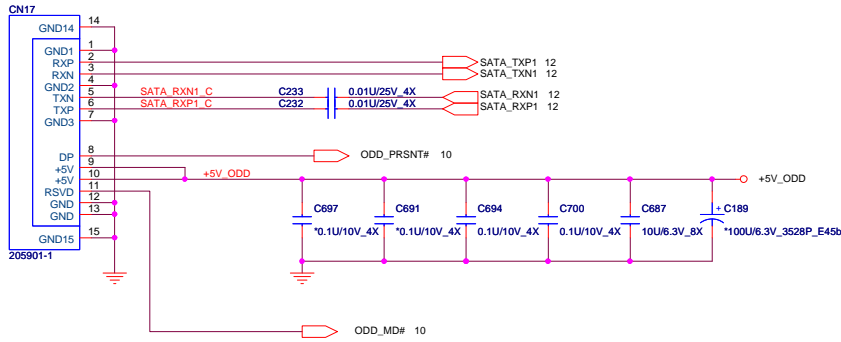
Quanta Computer Inc.

PROJECT : BLF_BLFD

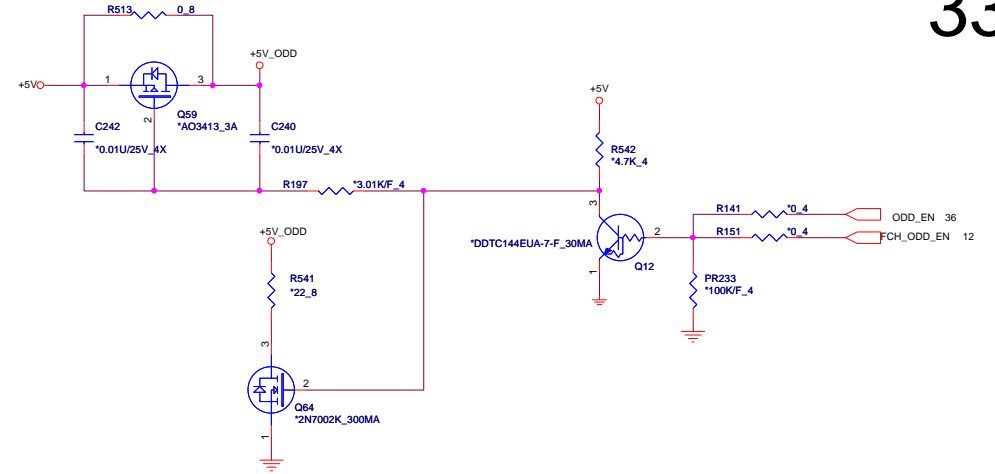
Size	Document Number	Rev
	BLANK	1C
Date:	Tuesday, April 19, 2011	Sheet 32 of 53

SATA ODD

[ODD]

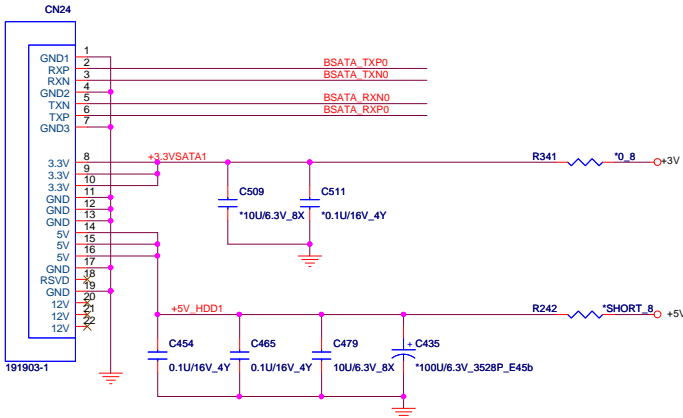


ODD Zero power .

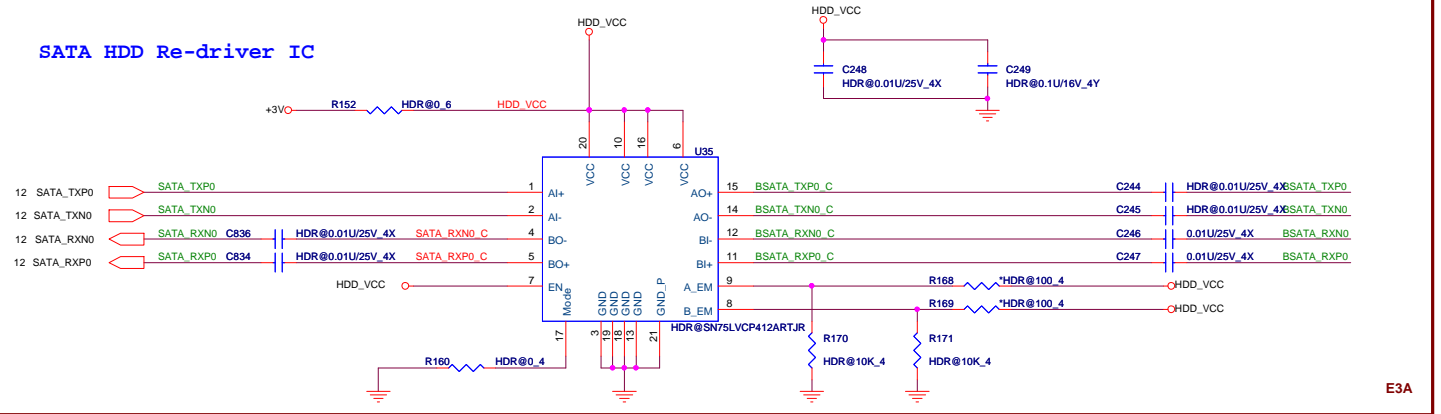


SATA HDD

[HDD]



SATA HDD Re-driver IC



Colay with Redriver IC SATA Re-driver Bypass

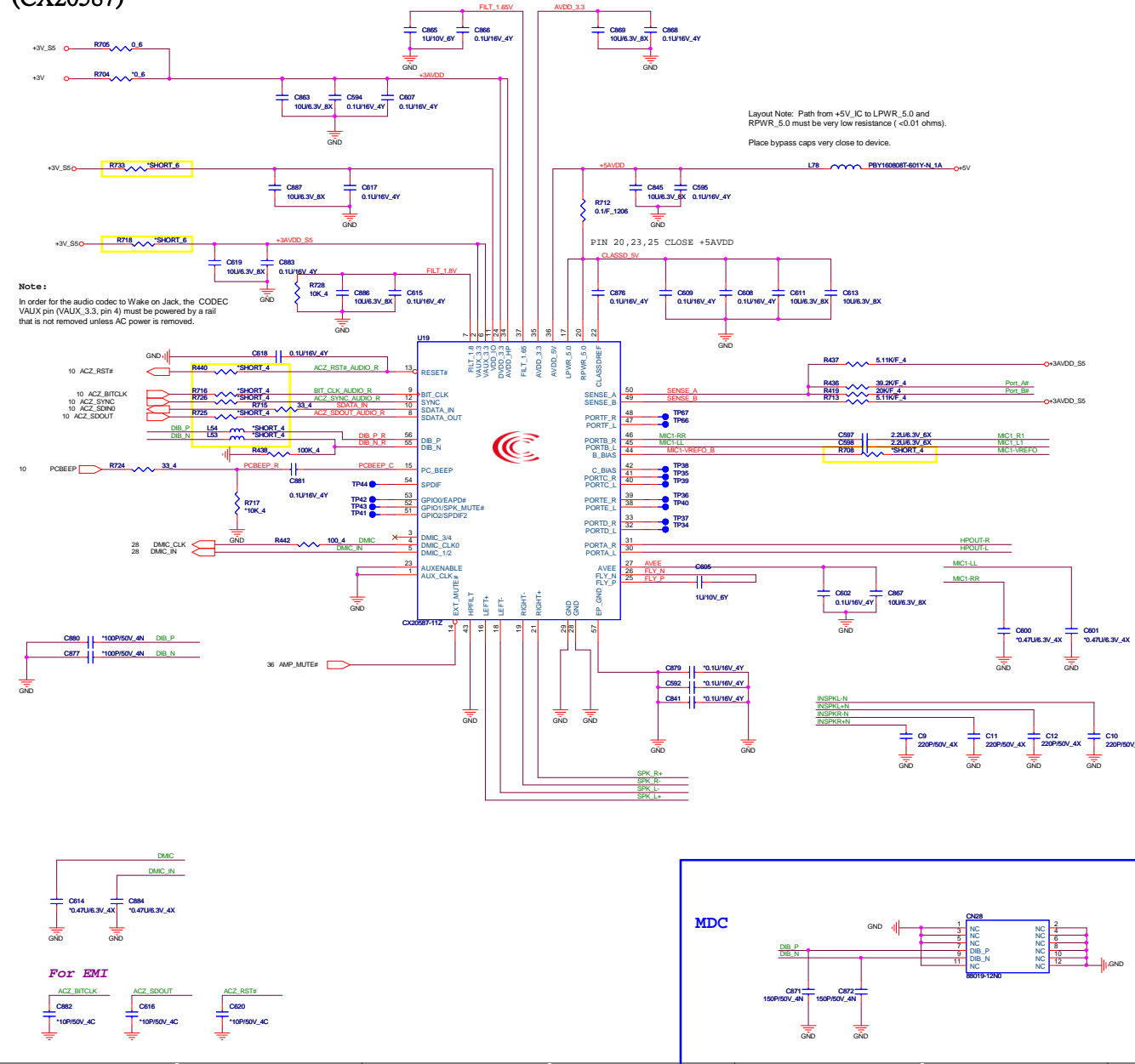
SATA_TXP0	R164	*0.4	BSATA_TXP0
SATA_TXN0	R165	*0.4	BSATA_TXN0
SATA_RXN0	R166	*0.4	BSATA_RXN0_C
SATA_RXP0	R167	*0.4	BSATA_RXP0_C

E3A

Quanta Computer Inc.
PROJECT : BLF_BLFD

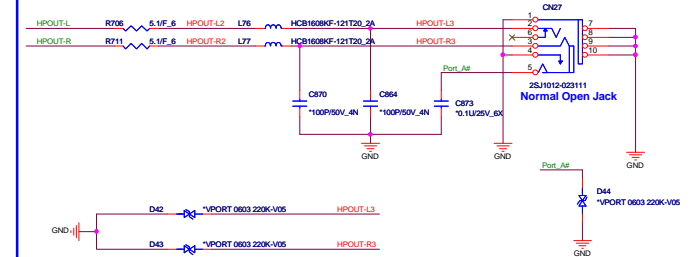
Size	Document Number	Rev
	HDD/ODD/MDC	1C
Date:	Tuesday, April 19, 2011	Sheet 33 of 53

Codec (CX20587)

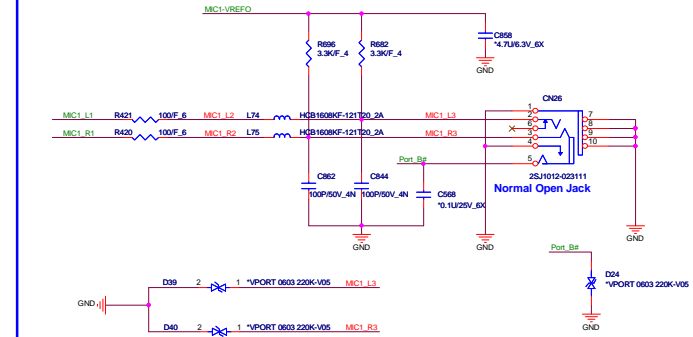


34

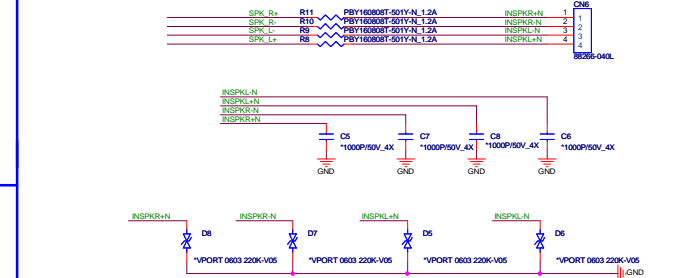
Earphone



External MIC

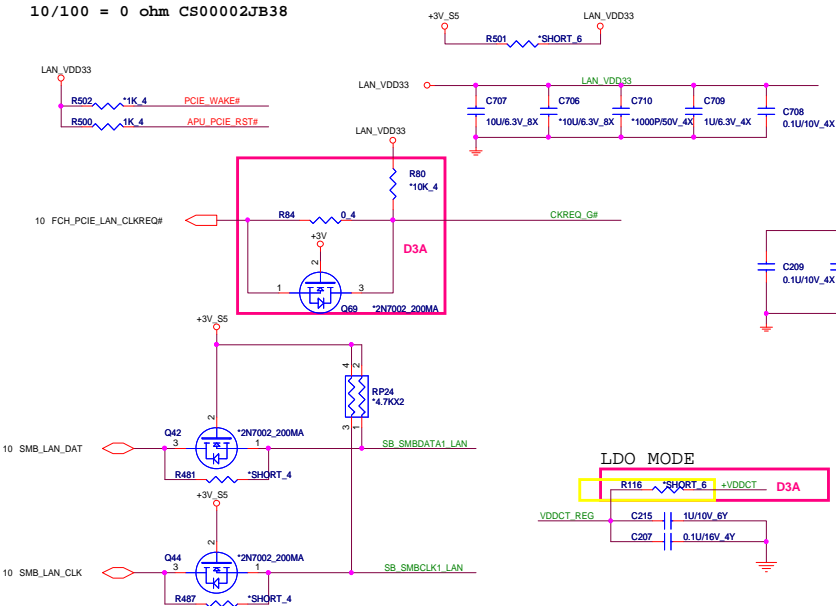


Internal Speaker

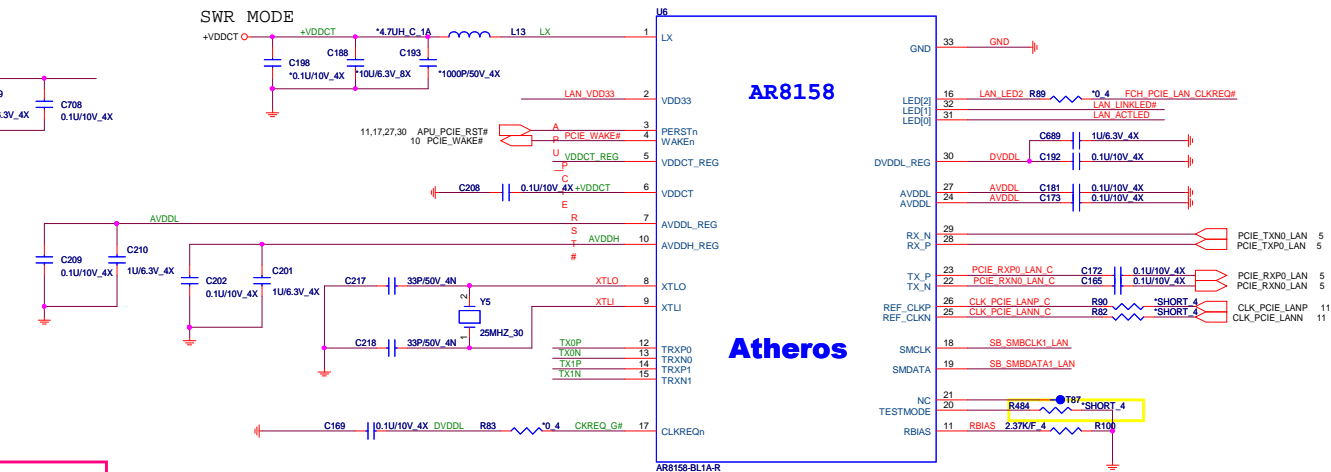
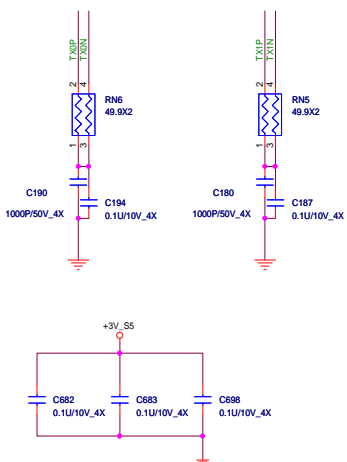


Atheros Lan AR8158

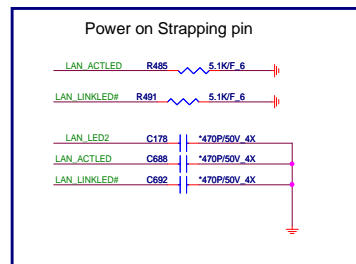
10/100 = 0 ohm CS00002JB38



PLACE NEAR LAN IC SIDE

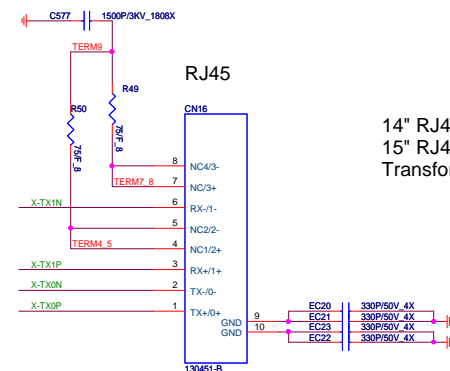
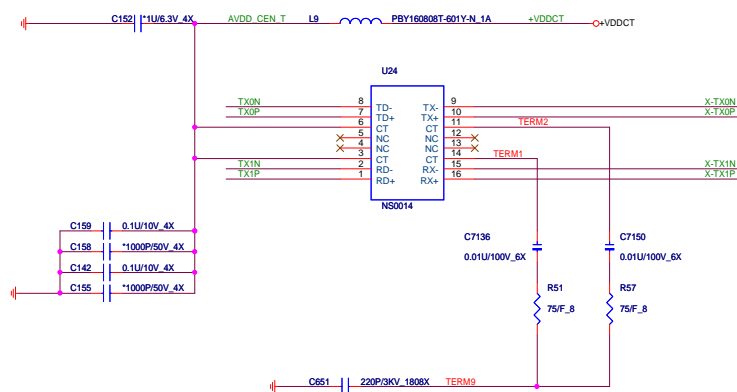


AMD 10/100: AR8158-BL1A-R = AL008158001

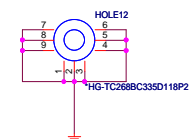


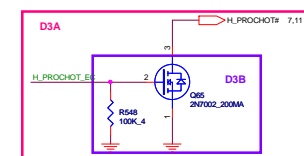
LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low

TRANSFORMER



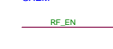
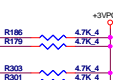
14" RJ45- DFTJ08FR164
15" RJ45- DFTJ08FR169
Transformer- DB0EL5LAN02





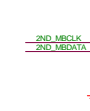
SMBUS Table

SMBUS	Devices	Address
1	Battery	
2	PCH SML1	
	3D Sensor	32H
	EC EEPROM	40H
3	VGA Board Thermal Sensor	98H
	Touch Sensor	58H
	HDMI CEC	34H
	Light Sensor	52H



SHBM=0: Enable shared memory with host BIOS
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

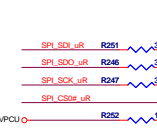
ID EEPROM



6 SCL A0 1 0.003A(20mils)

[illegible]

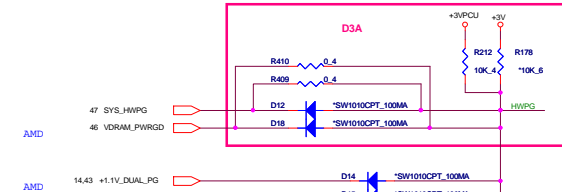
SPI
FLASH



MX25L3205DM2I-12G: AKE39FP0Z00
W25Q16BVSSIG: AKE39FP0N01

INTERNAL KEYBOARD STRIP
SET

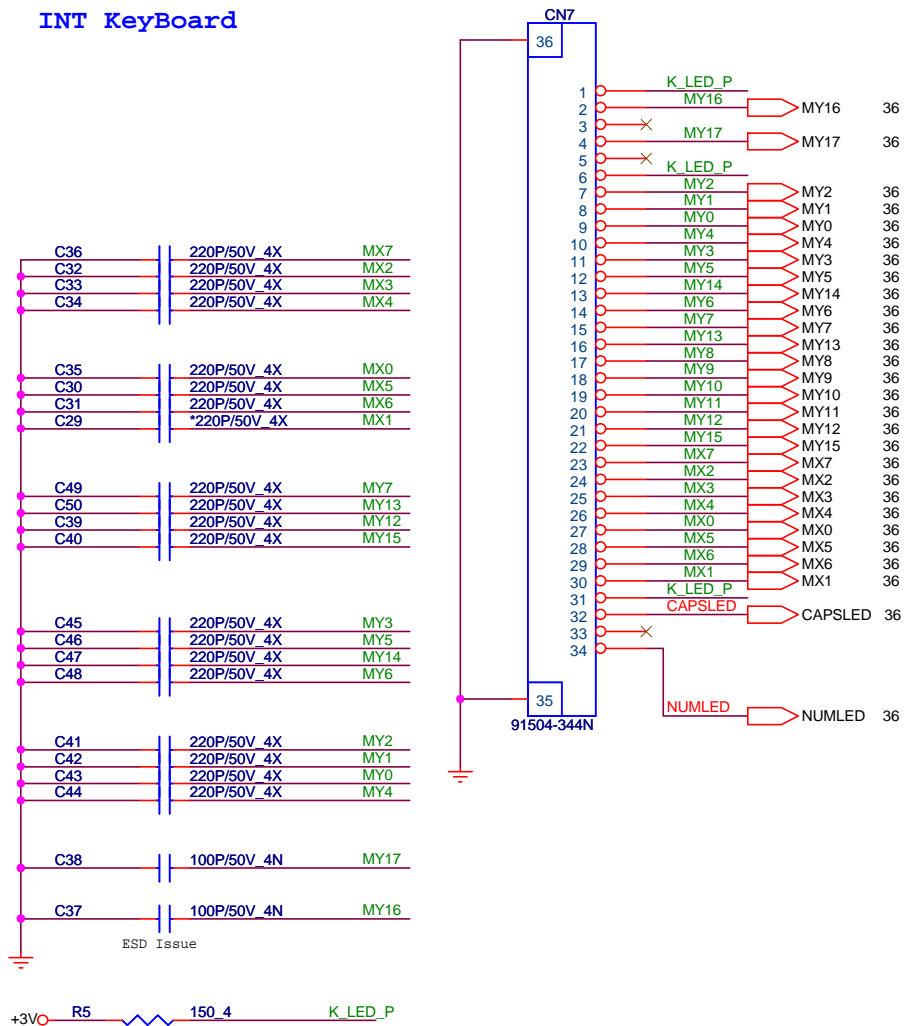
HWPG circuit



AMD

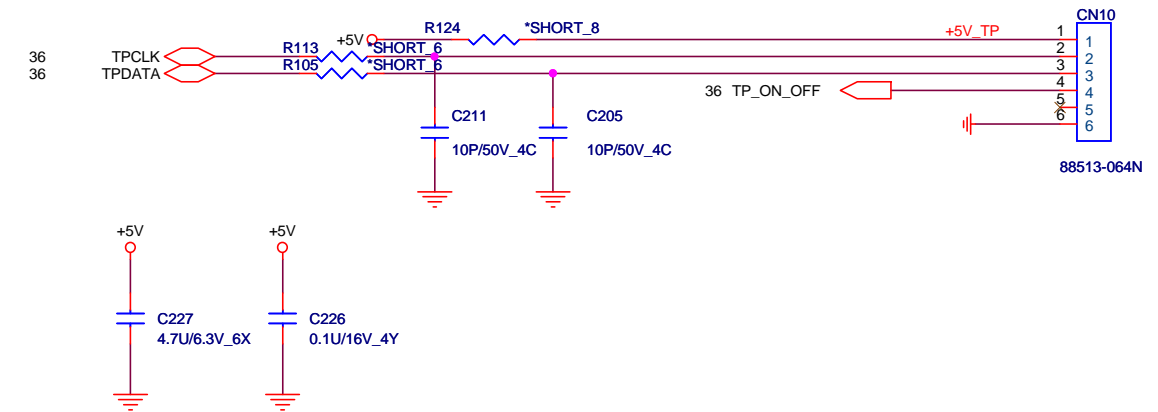
KEY BOARD Connector

INT KeyBoard

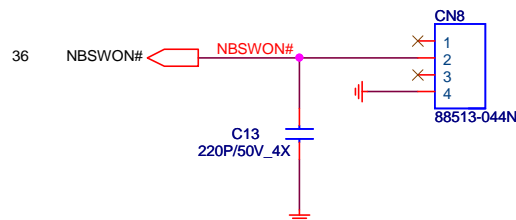


TOUCH PAD BOARD

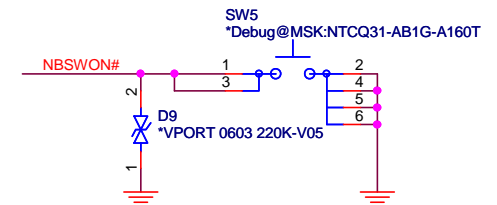
37



Power Board (UIF)



Power Switch (debug only)



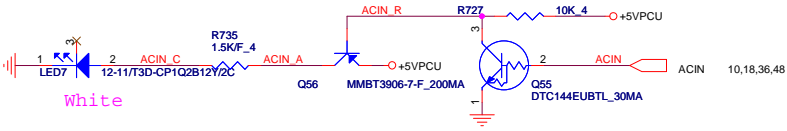
Quanta Computer Inc.

PROJECT : BLF_BLFD

Size	Document Number	Rev
	FP/TP/KB Conn	1C
Date:	Tuesday, April 19, 2011	Sheet 37 of 53

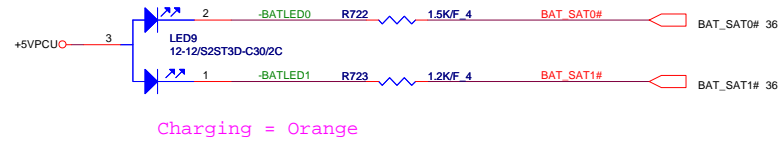
LED

AC-IN



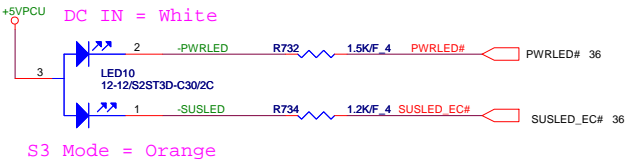
BATTERY

Full Charge = White



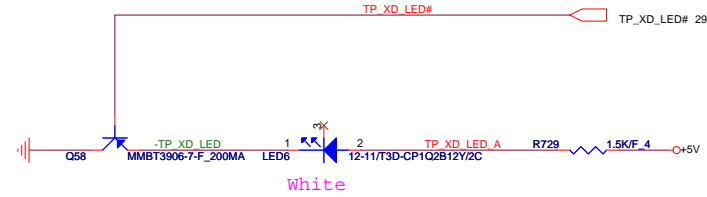
Charging = Orange

POWER



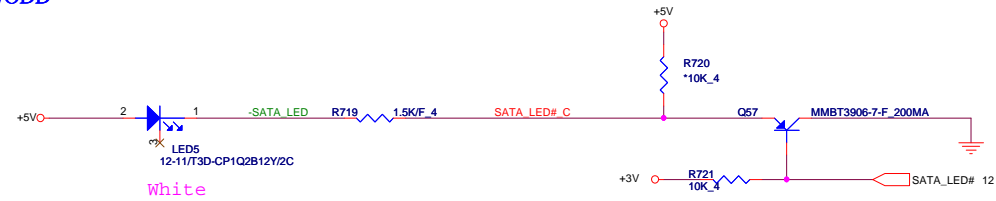
S3 Mode = Orange

CARDREADER



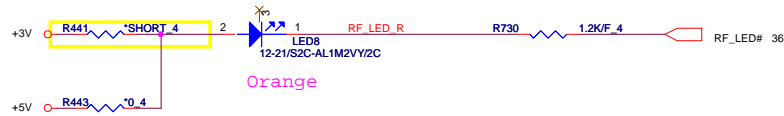
White

HDD/ODD



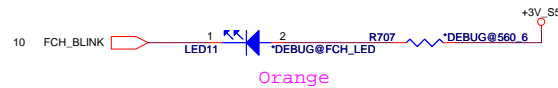
White

RF LED

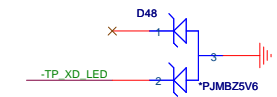
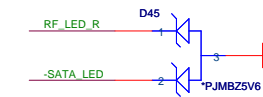
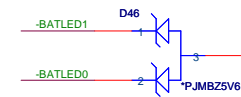
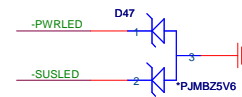


Orange

When ON, means in S0
When BLINK, means in S3
When OFF, means in S5



Orange



Quanta Computer Inc.

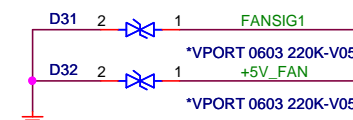
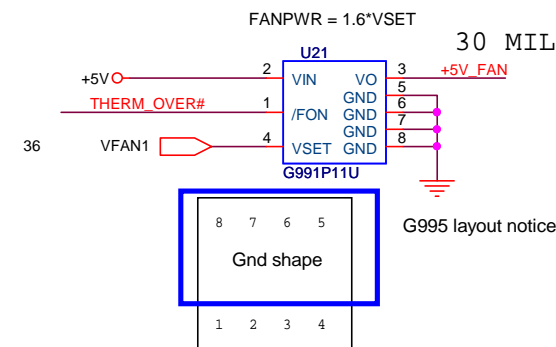
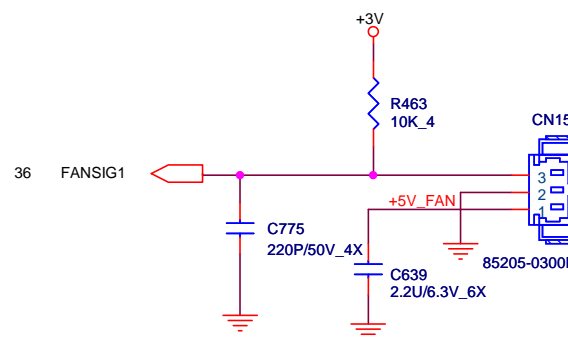
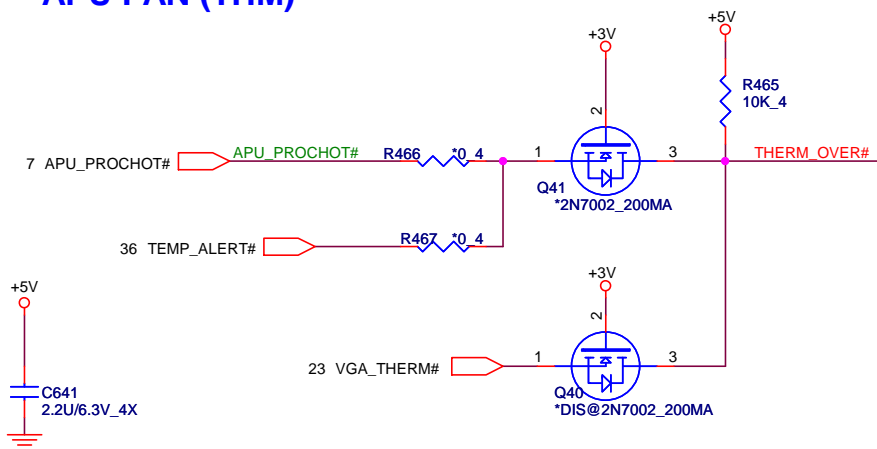
PROJECT : BLF_BLFD

Size	Document Number	Rev
	LED	1C
Date:	Tuesday, April 19, 2011	Sheet 38 of 53

1

APU FAN (THM)

39



Quanta Computer Inc.

PROJECT : BLF_BLFD

Size	Document Number	Rev
	APU FAN	1C
Date:	Tuesday, April 19, 2011	Sheet 39 of 53

D

D

C

C

B

B

A

A




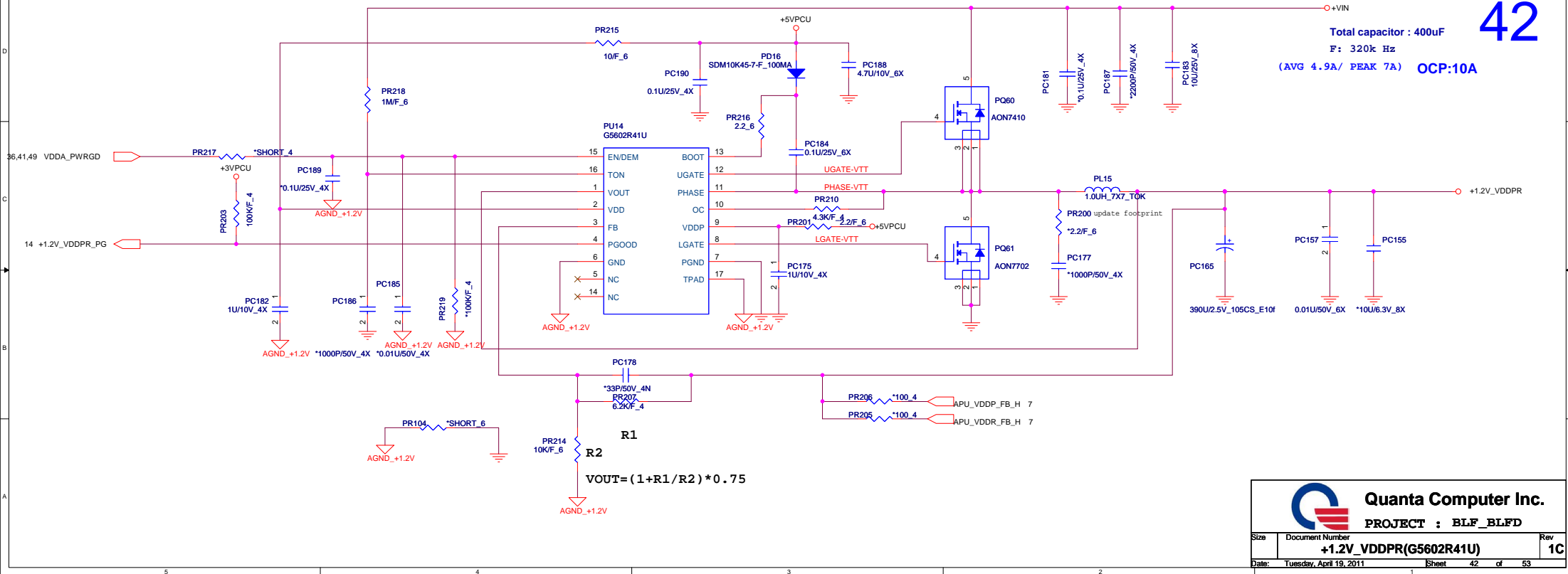
Quanta Computer Inc.

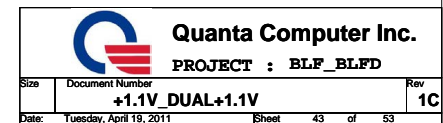
PROJECT : BLF_BLFD

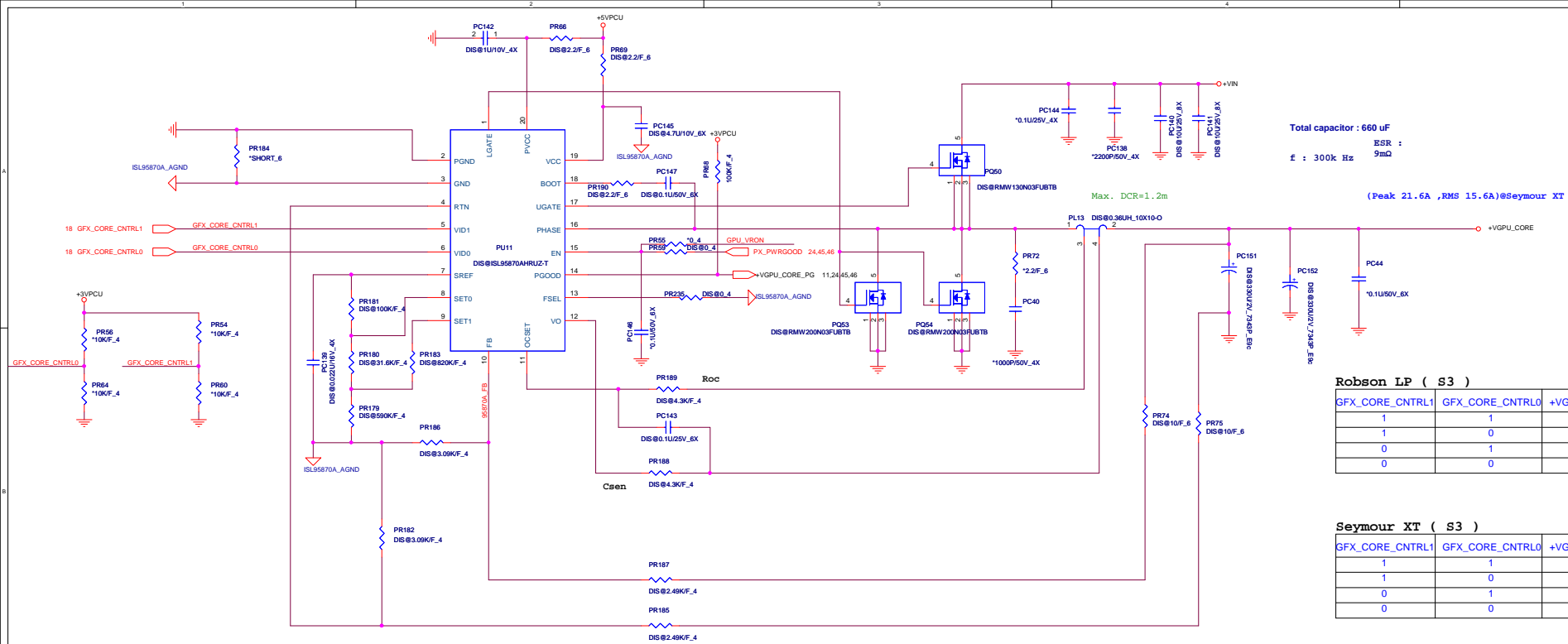
Size	Document Number	Rev
	BLANK	1C
Date:	Tuesday, April 19, 2011	Sheet 40 of 53



 <div> Quanta Computer Inc PROJECT : BLF_BLFD </div>	
Size	Document Number CPU CORE
Date	Tuesday, April 16, 2013 Sheet 41 of 63





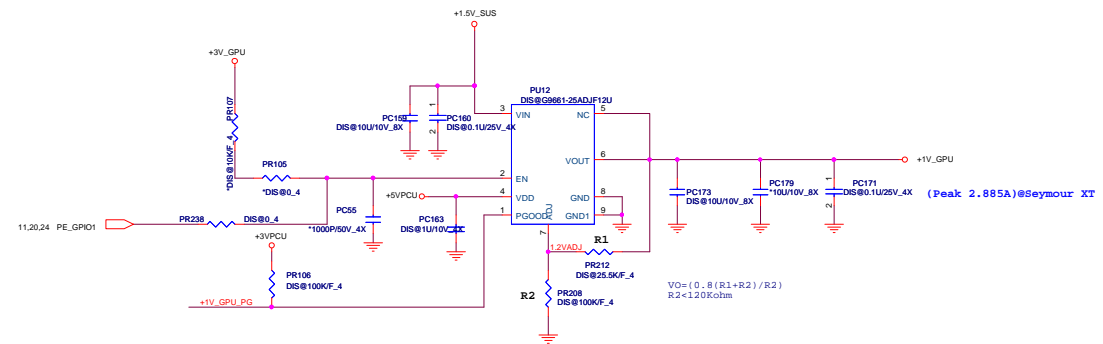


Robson LP (S3)	
------------------	--

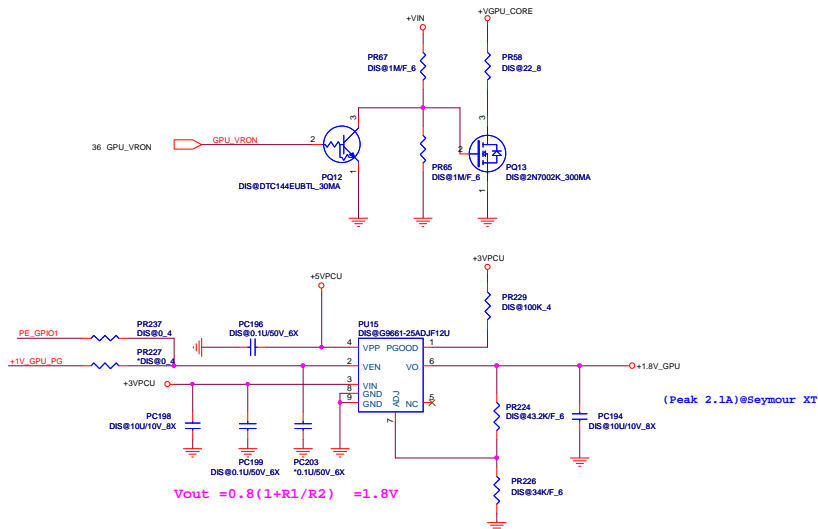
GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+VGPU_CORE
1	1	0.9V
1	0	0.95V
0	1	1.05V
0	0	1.12V

Seymour XT (S3)

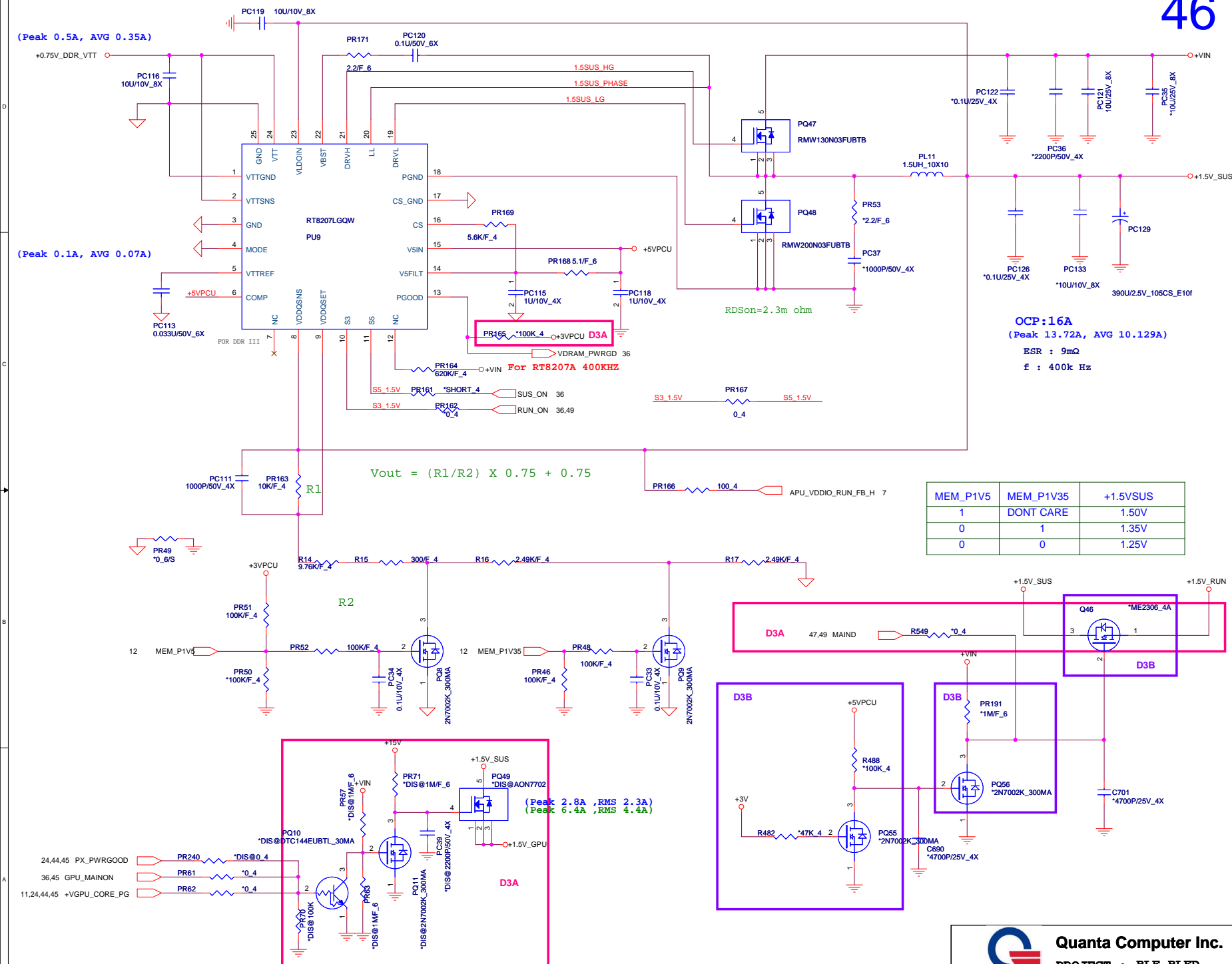
GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+VGPU_CORE
1	1	0.9V
1	0	1.05V
0	1	1.1V
0	0	1.15V

PCIE_VDDC
Madison, Park-->1.0V

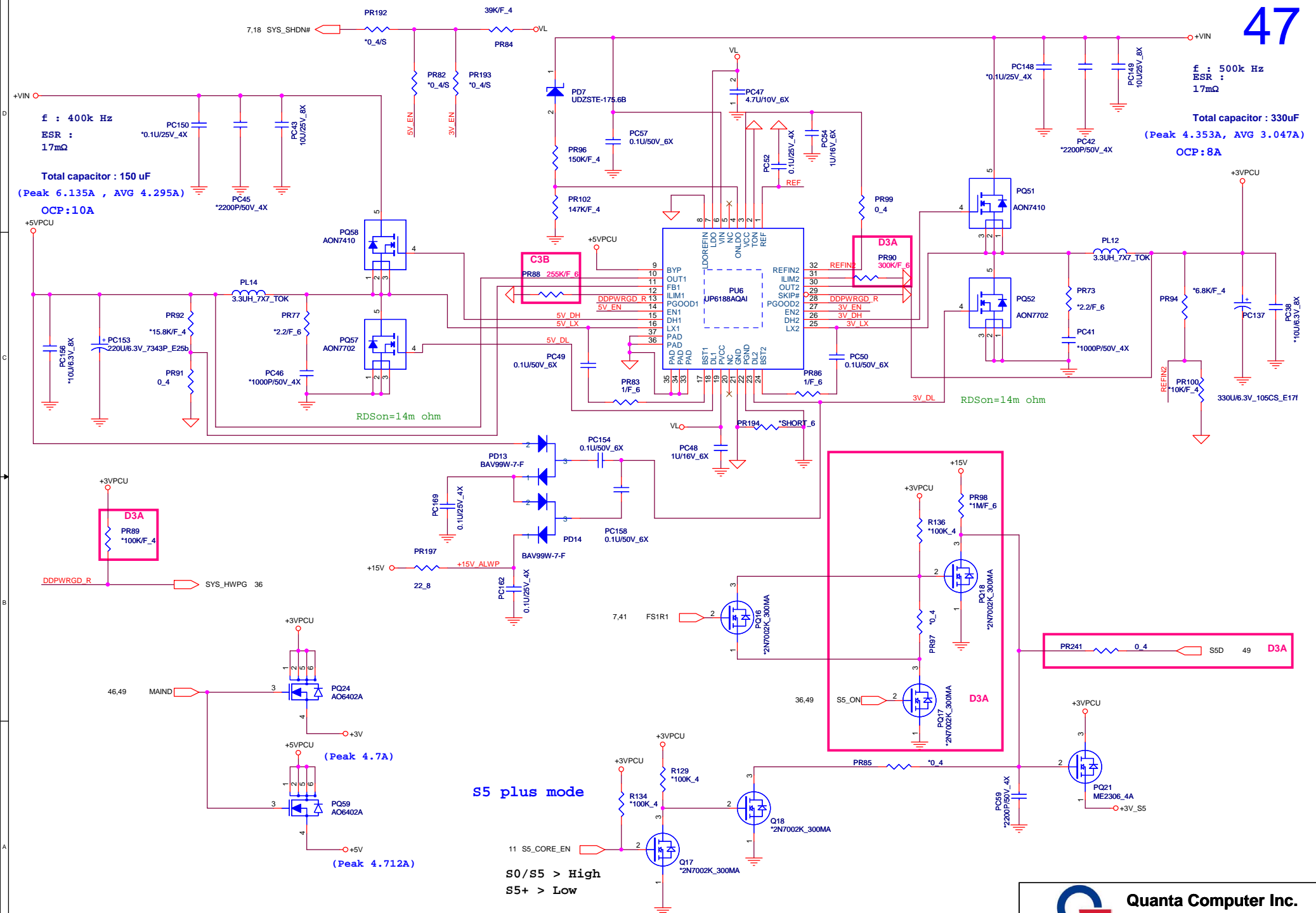
	Madison, Park
R1	25.5K/F_4 (CS32552FB11)
R2	100K/F_4 (CS41002FB28)

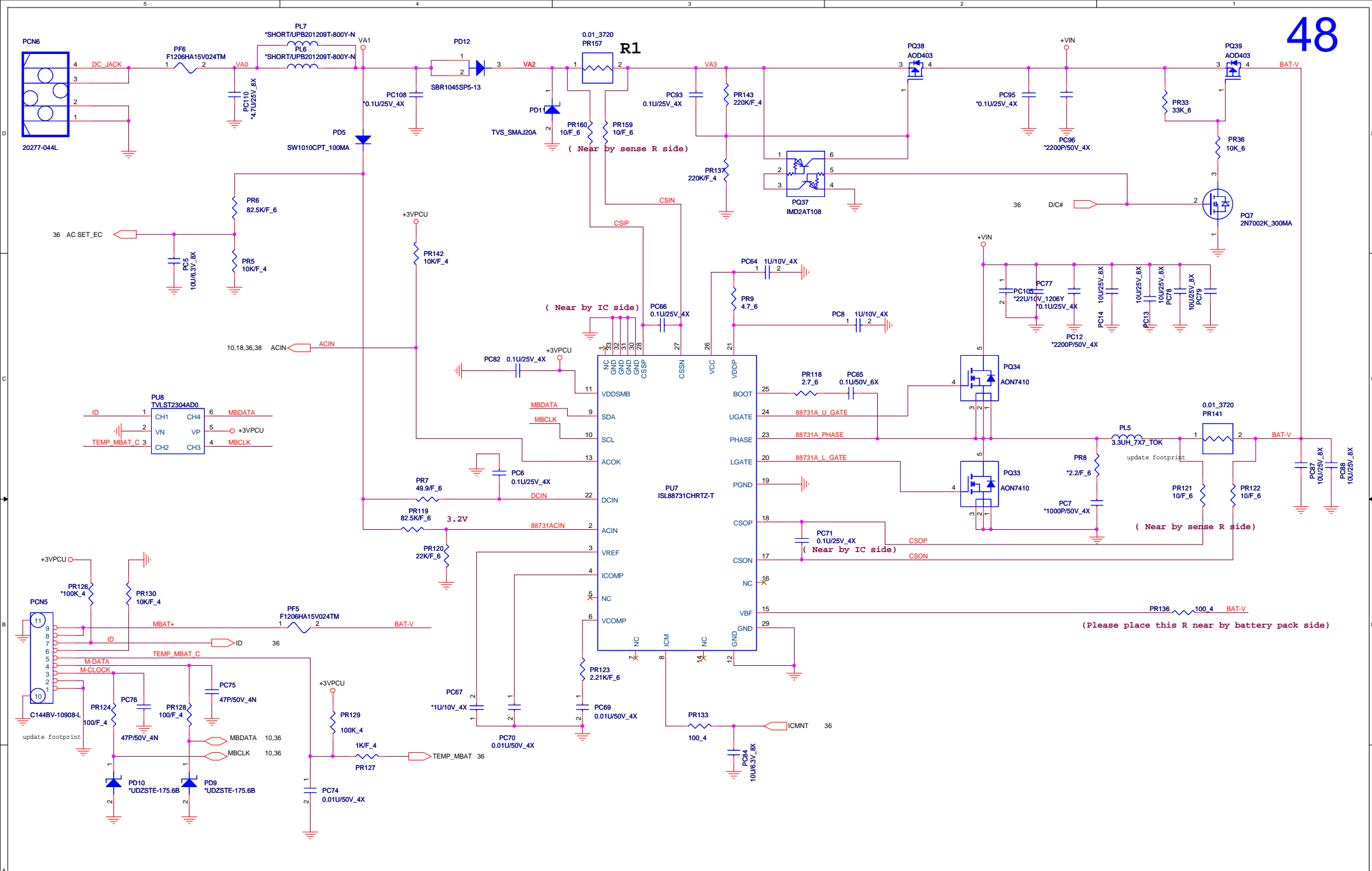


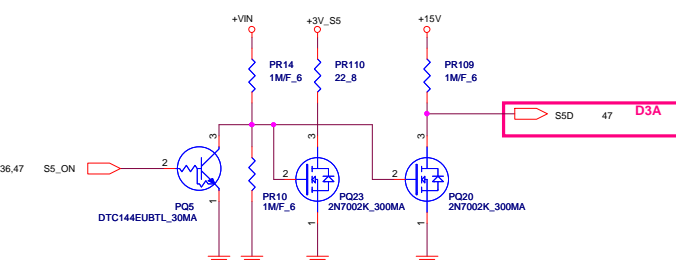




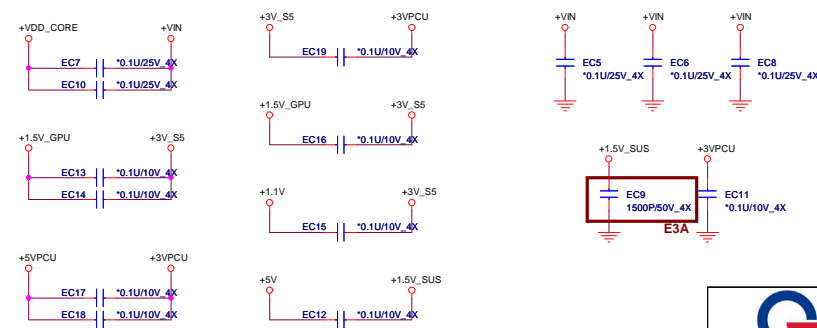
Total capacitor : 330uF
(Peak 4.353A, AVG 3.047A)
OCP: 8A

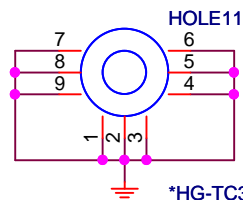




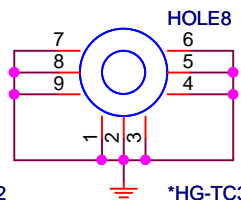


EMI

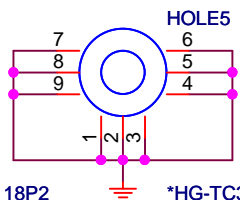




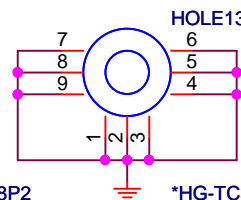
*HG-TC335BC268D118P2



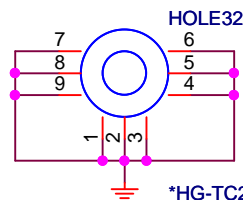
*HG-TC335BC268D118P2



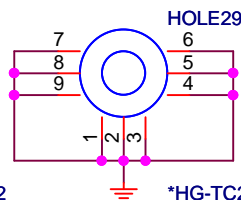
*HG-TC335BC268D118P2



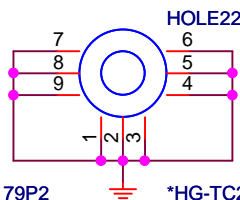
*HG-TC335BC268D118P2



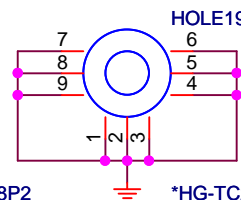
*HG-TC268BC335D118P2



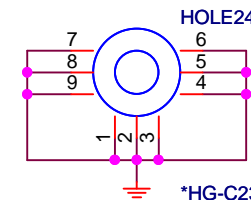
*HG-TC276BC335D179P2



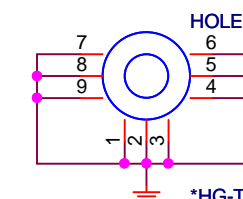
*HG-TC268BC335D118P2



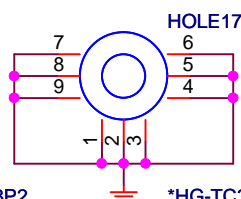
*HG-TC268BC335D118P2



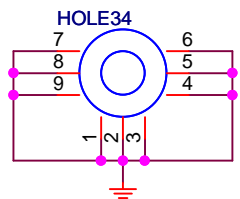
*HG-C236D146P2



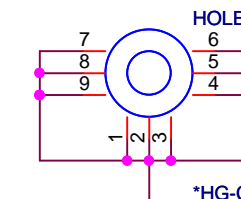
*HG-TC335BC268D118P2



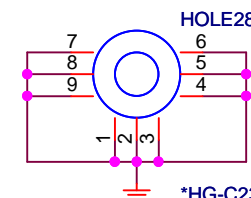
*HG-TC335BC268D118P2



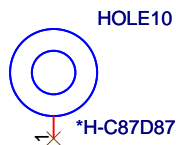
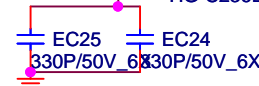
*HG-TC268BC335D118P2



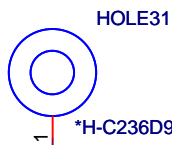
*HG-C236D118P2



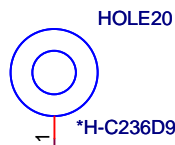
*HG-C236D146P2



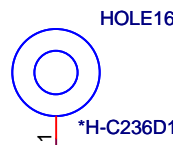
*H-C87D87N



*H-C236D91P2



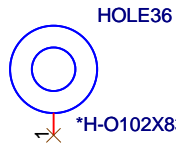
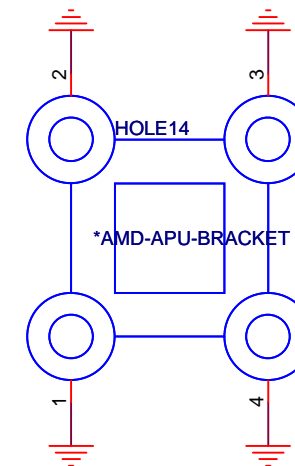
*H-C236D91P2



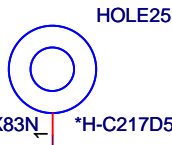
*H-C236D142P2



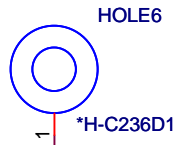
*H-C268D118P2



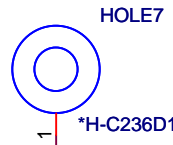
*H-O102X83D102X83N



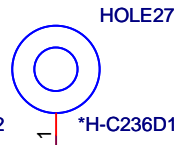
*H-C217D59P2



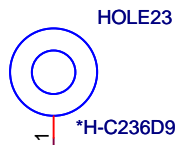
*H-C236D114P2



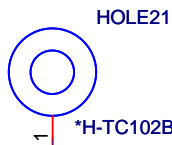
*H-C236D114P2



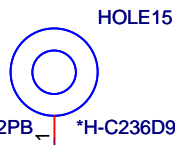
*H-C236D142P2



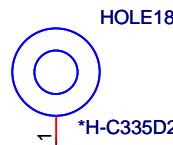
*H-C236D91P2



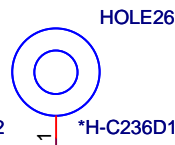
*H-TC102BC217D102PB



*H-C236D91P2



*H-C335D256P2



*H-C236D142P2



Quanta Computer Inc.

PROJECT : BLF_BLFD

Size	Document Number	Rev
	Screw	1C
Date:	Tuesday, April 19, 2011	Sheet 50 of 53